




Article

# Multibattery Charger System Based on a Multilevel Dual-Active-Bridge Power Converter

José M. Campos-Salazar <sup>1,\*</sup>, Sergio Busquets-Monge <sup>1</sup>, Alber Filba-Martinez <sup>1</sup> and Salvador Alepuz <sup>2</sup>

<sup>1</sup> Electronic Engineering Department, Universitat Politècnica de Catalunya, 08028 Barcelona, Spain; sergio.busquets@upc.edu (S.B.-M.); alber.filba@upc.edu (A.F.-M.)

<sup>2</sup> Tecnocampus, Universitat Pompeu Fabra, 08302 Mataró, Spain; alepuz@tecnocampus.cat

\* Correspondence: jose.manuel.campos@upc.edu

**Abstract:** This work introduces a novel battery charger implemented with a four-level three-phase neutral-point-clamped converter and a four-level single-phase dual-active-bridge converter, which offers the intrinsic advantages of multilevel conversion, provides galvanic isolation and allows bidirectional power flow. A detailed and extensive modeling of the system is developed, together with the design of appropriate closed-loop control and modulation. The proposed system allows individual charging of each battery pack, ensuring that the full capacity of the battery bank is utilized, even when the battery packs have different state-of-charge levels, differ in nominal capacities, or use different chemistries. Furthermore, the proposed control system manages the overall DC-link voltage and ensures voltage balance across both DC-links in the system. The effectiveness of the proposed system configuration and control has been validated through simulations. The simulation results show good dynamic response in different operating scenarios, confirming the suitability, feasibility, and benefits of the proposed implementation and control approach.

**Keywords:** DC-link voltage balancing; four-level battery charger; multibattery charging system



Academic Editor: Fabio Corti

Received: 10 March 2025

Revised: 12 April 2025

Accepted: 14 April 2025

Published: 19 April 2025

**Citation:** Campos-Salazar, J.M.; Busquets-Monge, S.; Filba-Martinez, A.; Alepuz, S. Multibattery Charger System Based on a Multilevel Dual-Active-Bridge Power Converter. *Electronics* **2025**, *14*, 1659. <https://doi.org/10.3390/electronics14081659>

**Copyright:** © 2025 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (<https://creativecommons.org/licenses/by/4.0/>).

## 1. Introduction

The role of batteries is becoming more and more important, given the technological evolution in recent years. With regard to the electric vehicle (EV), its rapid expansion [1,2] has intensified the demand for fast, efficient, and smart battery chargers, since the battery is the heart of the EV. Moreover, the use of smart bidirectional battery chargers enables the use of the energy stored in the batteries of the EV as a flexible energy storage unit in diverse applications, a system collectively known as vehicle-to-X [2–8], employed, for instance, to feed loads (vehicle-to-load, V2L) or to exchange energy with other vehicles (vehicle-to-vehicle, V2V), houses (vehicle-to-home, V2H), or the electric grid (vehicle-to-grid, V2G).

Batteries can also be applied to enhance the integration of renewable energy sources into the power network. Since the energy production of renewable energy sources obviously depends on the weather, a battery energy storage system (BESS) [9–11] can be used to store the energy surplus when more energy is produced than necessary, to be used at a later time when there is energy consumption but no energy production. To do it, the BESS requires a smart bidirectional battery charger.

In the context described above, battery chargers must deal with increasingly complex requirements, including the management of diverse battery chemistries [9], volt-

ages, and capacities, ensuring optimal performance in terms of efficiency, reliability, and adaptability [12,13], and meeting the corresponding standards [3,14].

Battery chargers have been extensively reported in the literature [2,3,15–19], where the most common approach is based on conventional two-level converters. Isolation is an usual requirement for battery chargers, which can be fulfilled by means of a bulky grid frequency transformer or preferably with a dual-active-bridge (DAB) converter [20], given its advantages of bidirectional power flow capability, soft-switching commutations, low cost, operational flexibility, and high efficiency [21]. DAB converters are particularly well suited for interfacing with EV charging stations and renewable energy storage systems, where operational flexibility and efficiency are critical [20].

Recent works [22–24] have demonstrated the feasibility and suitability of three-level DAB converters for battery charger applications. This topology offers the intrinsic advantages of a multilevel structure [25,26], voltage stress reduction on power semiconductors, harmonic distortion improvement, and converter efficiency increase together with improved voltage regulation and enhanced power quality, in comparison to the conventional two-level converters. These features are pivotal as EVs and renewable energy systems demand higher power densities, broader voltage ranges, and stricter efficiency targets.

The present work goes one step further and introduces a four-level battery charger (4L-BC) based on an extended DAB converter topology, which apparently has not been previously described in the literature. This manuscript presents a complete model of the system (switching model, large-signal averaged model, and small-signal linear model), together with the design of the proper modulation and closed-loop control. The proposed approach presents some significant characteristics, which are described below.

The four-level structure provides reduced voltage stress on semiconductor devices, leading to better reliability and longer component lifespans, and smaller harmonic distortion, resulting in improved power quality and reduced electromagnetic interference [26,27].

The closed-loop control and modulation algorithms play a key role in the proposed system. For the grid-side converter, power factor control, a low harmonic distortion of the grid current, and DC-link capacitor voltage balance [28] are achieved. For the DAB converter, the charge/discharge current across each battery pack can be precisely controlled [27].

This last feature is particularly relevant. Since the charge/discharge current can be particularized for each battery pack, this can be extremely useful in the case of heterogeneous batteries with different state-of-charge (SoC), chemistries, or capacities [29–31]. The proposed system allows for the efficient and independent regulation for each battery, optimizing the overall charging and discharging process and ensuring a proper SoC balance across the battery packs [27]. The ability to handle batteries with different SoCs is essential for achieving optimal energy utilization and prolonging battery lifespans.

In summary, this work contributes to the ongoing development of multibattery charging systems by offering a comprehensive analysis of the four-level DAB converter capabilities. Through detailed analysis and simulation, this study validates the 4L-BC as a possible solution for next-generation battery charging applications.

This manuscript is structured as follows: Section 2 introduces the proposed charger topology, highlighting its design features. Sections 3–5 develop the switching model, large-signal averaging model, and small-signal linear model, respectively. Section 6 describes the control system design and the modulation algorithms and provides the system transfer functions. Section 7 presents the system stability analysis and the time-domain simulation results, offering insights into system behavior under various operating conditions. Finally, Section 8 concludes the manuscript by summarizing the key findings and contributions.

## 2. Battery Charger Topology

Figure 1 illustrates the topology and circuit model of the proposed 4L-BC in detail. It is worth mentioning that the system described in Figure 1 is bidirectional, that is, power can flow from the grid to the batteries and vice versa. The system is connected to the three-phase AC grid through an inductive filter and an AC-DC conversion stage. This stage employs a four-level neutral-point-clamped (NPC) converter [26], identified as 4L-3P-NPC converter in Figure 1, which performs the AC-DC conversion between the AC grid and the a-side DC-link.

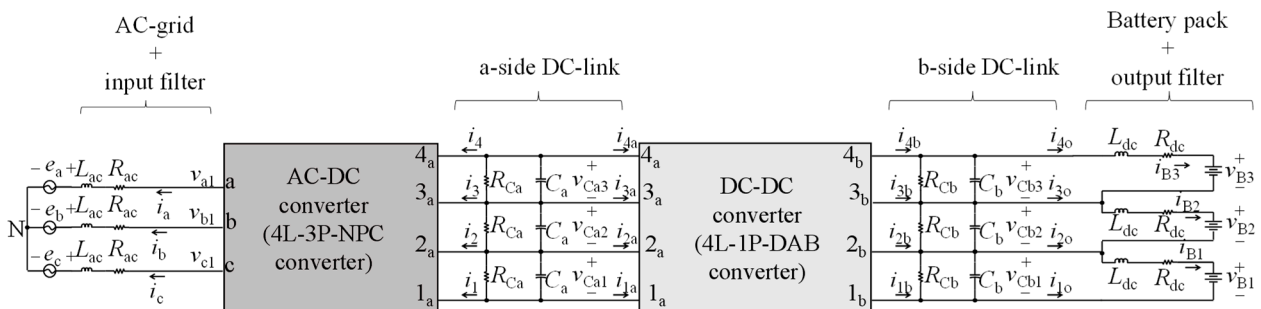


Figure 1. Four-level battery charger topology.

The DC-DC conversion stage between the a-side DC-link and the b-side DC-link is implemented by using a four-level single-phase dual-active-bridge (4L-1P-DAB) converter [25] integrated with a high-frequency transformer (HFT). This converter guarantees efficient power conversion and galvanic isolation between both DC-link sides. Capacitors  $C_a$  and  $C_b$  on the a-side and b-side, respectively, with parallel resistors  $R_{Ca}$  and  $R_{Cb}$ , ensure voltage stability and dissipate excess energy to prevent overvoltage [23].

The battery bank consists of three battery packs, which are connected between the voltage levels  $1_b-2_b$ ,  $2_b-3_b$ , and  $3_b-4_b$  of the b-side DC-link, respectively, as depicted in Figure 1.

## 3. Battery Charger Switching Model

The development of the switching model for the 4L-BC involves the modeling of the 4L-3P-NPC converter, the 4L-1P-DAB converter, and the battery bank. Each component is analyzed individually to describe their switching dynamics across varying operational states.

The 4L-3P-NPC converter model describes the interaction among the voltages and currents of the AC grid and the a-side DC-link through the switching states of the converter. For the 4L-1P-DAB converter, the model includes the dynamics of the HFT and the b-side DC-link, with an emphasis on switching event timing to regulate power flow between the b-side DC-link and the battery bank [32,33]. The battery bank model reflects the electrical characteristics of each individual battery pack and their combined response to charging currents determined by converter operation.

This component-wise modeling provides a comprehensive switching model for the entire 4L-BC system, facilitating the understanding of component interactions and enabling control strategy optimization for enhanced performance and efficiency.

### 3.1. 4L-3P-NPC Converter Switching Model

Figure 2 illustrates the switching model of the 4L-3P-NPC converter. AC grid voltages (with respect to N) are denoted as  $e_a$ ,  $e_b$ , and  $e_c$ , AC grid currents as  $i_a$ ,  $i_b$ , and  $i_c$ , and the voltages at the AC port of the converter (with respect to DC-rail  $1_a$ ) as  $v_{a1}$ ,  $v_{b1}$ , and  $v_{c1}$ . The capacitor voltages  $C_a$  are represented by  $v_{Ca1}$ ,  $v_{Ca2}$ , and  $v_{Ca3}$ , with corresponding a-side DC-link currents  $i_1$ ,  $i_2$ ,  $i_3$ , and  $i_4$ . Additionally,  $i_{1a}$ ,  $i_{2a}$ ,  $i_{3a}$ , and  $i_{4a}$  denote the currents

flowing from the 4L-3P-NPC converter into the 4L-1P-DAB converter, as shown in Figure 2. The parameters  $R_{ac}$  and  $L_{ac}$  represent the AC grid filter resistor and inductor values, while  $R_{Ca}$  and  $C_a$  indicate the bleeding resistors and capacitors of the a-side DC-link.

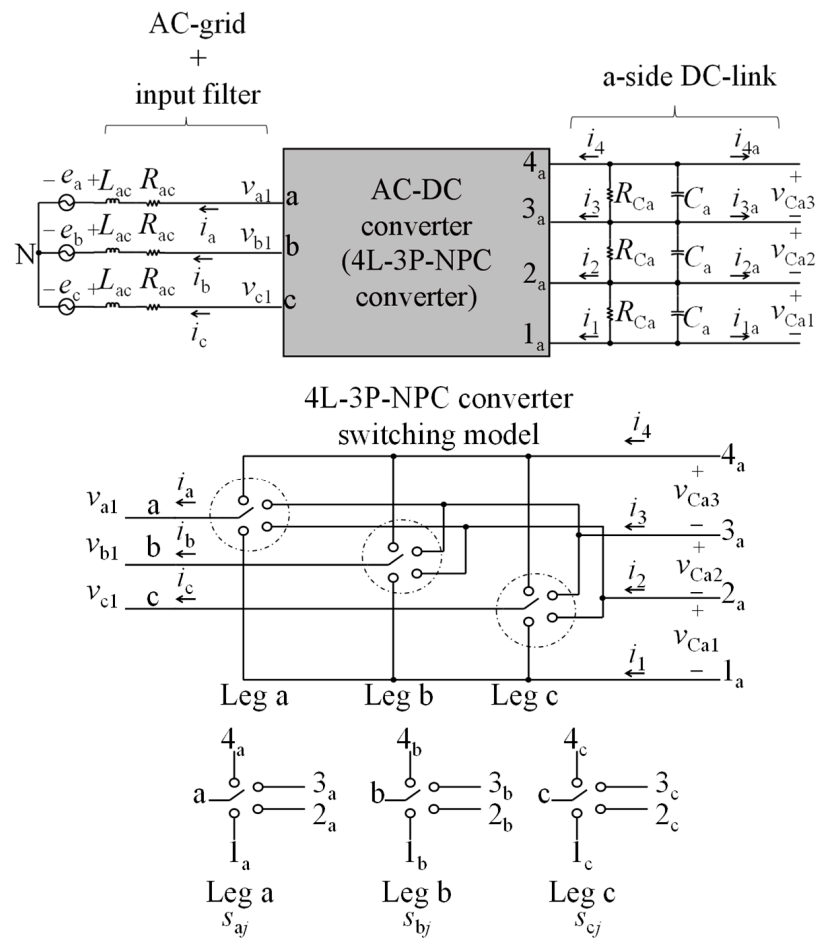


Figure 2. Switching model of the 4L-3P-NPC converter.

The developed model for the 4L-3P-NPC converter provides the equations for the AC grid and the a-side DC-link. These equations, obtained from Figure 2, are presented as follows:

$$\frac{dx_1}{dt} = \mathbf{A}_1(t) \cdot \mathbf{x}_1 + \mathbf{B}_1 \cdot \mathbf{u}_1 \tag{1}$$

where  $\mathbf{x}_1 = [i_a, i_b, i_c, v_{Ca1}, v_{Ca2}, v_{Ca3}]^T$  and  $\mathbf{u}_1 = [e_a, e_b, e_c, i_{2a}, i_{3a}, i_{4a}]^T$ . Symbolically,  $\{\mathbf{x}_1, \mathbf{u}_1\} \in \{\mathbb{R}^6\}$ . The switching functions in (1) are defined by:

$$s_{ij} = \begin{cases} 1, & i \text{ connected to } j \\ 0, & \text{else} \end{cases} \tag{2}$$

$$s_{i1a} + s_{i2a} + s_{i3a} + s_{i4a} = 1 \tag{3}$$

for  $i \in \{a, b, c\}$  and  $j \in \{1_a, 2_a, 3_a, 4_a\}$ . The model in (1) is discrete and nonlinear, due to the inclusion of the switching functions within the state matrix  $\mathbf{A}_1(t)$ , as developed in [20]. The state matrix  $\mathbf{A}_1(t)$  and the input matrix  $\mathbf{B}_1$  are defined in Appendix A.

### 3.2. 4L-1P-DAB Converter Switching Model

Figure 3 provides a comprehensive switching model of the 4L-1P-DAB converter. In this model, the primary and secondary side input currents of the HFT are denoted as  $i_{aT}$

and  $i_{bT}$ , respectively, and the magnetizing current is represented by  $i_{mT}$ . The input terminal voltages on the HFT's primary and secondary sides are labeled as  $v_{aT}$  and  $v_{bT}$ , respectively. Parameters  $R_{Lk}$ ,  $L_k$ ,  $L_m$ , and  $a_{tr}$  correspond to the resistance and leakage inductance of the HFT windings, the magnetizing inductance, and the turn ratio ( $a_{tr} = 1/n$ ) of the HFT, respectively. The relationship between leakage and magnetizing inductance is expressed as  $L_k \parallel L_m = L_m \cdot L_k / L_k + L_m$ , reflecting the parallel combination in the equivalent circuit.

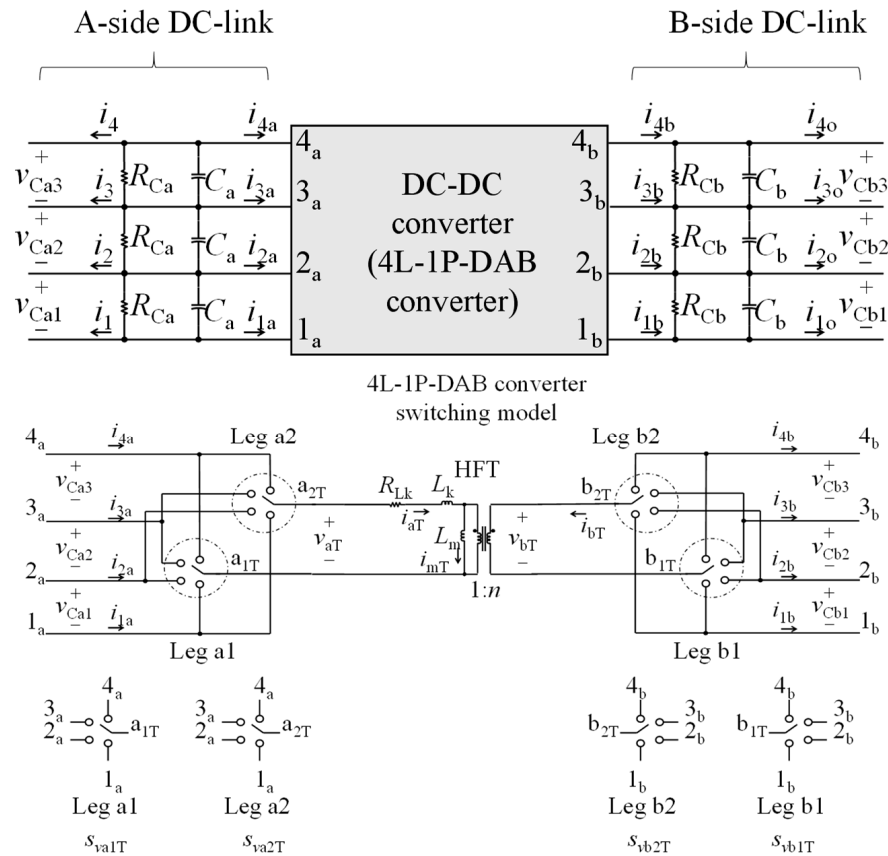


Figure 3. Switching model of the 4L-1P-DAB converter.

The b-side DC-link voltages across capacitors are denoted by  $v_{Cb1}$ ,  $v_{Cb2}$ , and  $v_{Cb3}$ . The currents through the b-side DC-link,  $i_{1b}$ ,  $i_{2b}$ ,  $i_{3b}$ , and  $i_{4b}$ , correspond to the currents entering the battery bank, while  $i_{1o}$ ,  $i_{2o}$ ,  $i_{3o}$ , and  $i_{4o}$  are the currents directly flowing through the battery bank.

The model also incorporates the capacitors  $C_b$  and the bleeding resistors  $R_{Cb}$  of the b-side DC-link. This switching model describes the dynamic behavior of the 4L-1P-DAB converter, emphasizing its interaction with the battery bank and detailing the complex interplay between converter components and the battery storage system.

Based on the configuration in Figure 3, the switching model of the 4L-1P-DAB converter is presented in the following:

$$\frac{dx_2}{dt} = \mathbf{A}_2(t) \cdot \mathbf{x}_2 + \mathbf{B}_2 \cdot \mathbf{u}_2 \tag{4}$$

where  $\mathbf{x}_2 = [v_{Ca1}, v_{Ca2}, v_{Ca3}, i_{aT}, i_{mT}, i_{bT}, v_{Cb1}, v_{Cb2}, v_{Cb3}]^T$  and  $\mathbf{u}_2 = [i_2, i_3, i_4, i_{2o}, i_{3o}, i_{4o}]^T$ . Symbolically,  $\mathbf{x}_2 \in \{\mathbb{R}^9\}$  and  $\mathbf{u}_2 \in \{\mathbb{R}^6\}$ . Matrices  $\mathbf{A}_2(t)$  and  $\mathbf{B}_2$  are defined in Appendix A, as in the case of the 4L-3P-NPC converter. In this converter, the state matrix  $\mathbf{A}_2(t)$  is also

time-varying, mainly due to the presence of the switching functions. The corresponding switching functions of the converter are defined as follows:

$$s_{vw} = \begin{cases} 1, & v \text{ connected to } w \\ 0, & \text{else} \end{cases}, \text{ where} \tag{5}$$

$$v \in \{1_a, 2_a, 3_a, 4_a, 1_b, 2_b, 3_b, 4_b\}, w \in \{a_{1T}, a_{2T}, b_{1T}, b_{2T}\}$$

$$s_{1aw} + s_{2aw} + s_{3aw} + s_{4aw} = 1 \tag{6}$$

$$s_{1bw} + s_{2bw} + s_{3bw} + s_{4bw} = 1 \tag{7}$$

### 3.3. Battery Bank Model

The configuration of the battery bank within the 4L-BC system is detailed in Figure 4. The battery bank consists of three battery packs connected to the b-side DC-link, with its mathematical model given by:

$$\frac{d\mathbf{i}_B}{dt} = -\frac{R_{dc}}{L_{dc}} \cdot \mathbf{I}_3 \cdot \mathbf{i}_B + \frac{1}{L_{dc}} \cdot \mathbf{B}_3 \cdot \mathbf{v} \tag{8}$$

where  $\mathbf{i}_B = [i_{B1}, i_{B2}, i_{B3}]^T$  and  $\mathbf{v} = [v_{Cb1}, v_{Cb2}, v_{Cb3}, v_{B1}, v_{B2}, v_{B3}]^T$ . Symbolically,  $\mathbf{i}_B \in \{\mathbb{R}^3\}$  and  $\mathbf{v} \in \{\mathbb{R}^6\}$ . In addition,  $\mathbf{I}_3$  is the  $3 \times 3$  identity matrix and  $\mathbf{B}_3$  is defined in Appendix A. Also,  $i_{B1}$ ,  $i_{B2}$ , and  $i_{B3}$  denote the charging currents, while  $v_{B1}$ ,  $v_{B2}$ , and  $v_{B3}$  represent the terminal voltages of the respective battery packs.

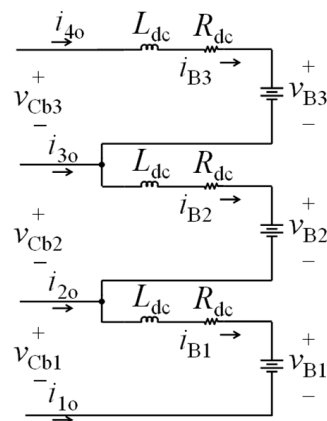


Figure 4. Four-level battery bank model.

The inductance  $L_{dc}$  and resistance  $R_{dc}$  of the wires affect the transient and steady-state behavior of the system during the charging process. Each battery pack in the bank is modeled using a Thévenin equivalent circuit [29,30], which incorporates a voltage source representing the open-circuit voltage of the battery, indicative of its state of charge.

## 4. Large-Signal Averaged Model

The large-signal averaged models of the three main components of the 4L-BC system are presented in this section: the 4L-3P-NPC converter, the 4L-1P-DAB converter, and the battery bank. These models help to analyze the dynamic behavior of the 4L-BC system under different operating conditions, providing a macroscopic view by smoothing out high-frequency switching effects and aiding in control algorithm design [32,33].

The 4L-3P-NPC converter model describes the interactions between the AC grid and DC-link, while the 4L-1P-DAB converter model details the HFT operation. The battery bank model accounts for electrochemical characteristics and charge/discharge cycles [27]. These

averaged models support developing control strategies to improve efficiency, stability, and energy management.

Classical control theory uses continuous-time representations, requiring an averaging operator to convert discrete switching signals into continuous duty ratios. The averaging operator is defined as follows:

$$\langle x \rangle_{T_s} = \frac{1}{T_s} \cdot \int_{t-T_s}^t x(\tau) d\tau \tag{9}$$

To ensure accurate correlation between actual and averaged values, the switching frequency  $f_s$  must be significantly higher than the AC grid fundamental frequency  $f_o$ . In this work, a 10 kHz frequency is used for both converters, which is higher than the 50 Hz grid frequency.

Applying this averaging process enables developing continuous-time models for effective control system design, bridging the gap between the discrete nature of power electronics and the classical control methodologies.

#### 4.1. 4L-3P-NPC Converter Large-Signal Averaged Model

The averaging operator defined in (9) is applied to the switching model of the converter, as detailed in (1). The Park transformation then provides the large-signal averaged model in the D-Q reference frame. The resulting compact differential equation is given by:

$$\frac{d\langle v_{C_{a_i}} \rangle_{T_s}}{dt} = -\frac{1}{C_a} \cdot \left[ \frac{\langle v_{C_{a_i}} \rangle_{T_s}}{R_{C_a}} + \sum_{j \neq i} \frac{\langle v_{C_{a_i}} \rangle_{T_s} \cdot \langle i_{2_j} \rangle_{T_s}}{\sum_{k=1}^3 \langle v_{C_{a_k}} \rangle_{T_s}} + \frac{\langle v_{C_{a_m}} \rangle_{T_s} \cdot \langle i_{3_j} \rangle_{T_s}}{\sum_{k=1}^3 \langle v_{C_{a_k}} \rangle_{T_s}} + \sum_{n=2}^4 \langle i_{n_a} \rangle_{T_s} + \frac{\langle v_d \rangle_{T_s} \cdot \langle i_d \rangle_{T_s} + \langle v_q \rangle_{T_s} \cdot \langle i_q \rangle_{T_s}}{\sum_{k=1}^3 \langle v_{C_{a_k}} \rangle_{T_s}} \right], \text{ here } \{i, j, k\} \in \{1, 2, 3\}, j \neq i, m \neq i \neq j \tag{10}$$

The resulting model consists of five state variables,  $\langle i_d \rangle_{T_s}$ ,  $\langle i_q \rangle_{T_s}$ ,  $\langle v_{C_{a1}} \rangle_{T_s}$ ,  $\langle v_{C_{a2}} \rangle_{T_s}$ , and  $\langle v_{C_{a3}} \rangle_{T_s}$ , and six input variables,  $\langle i_{2_1} \rangle_{T_s}$ ,  $\langle i_{3_1} \rangle_{T_s}$ ,  $\langle i_{2_a} \rangle_{T_s}$ ,  $\langle i_{3_a} \rangle_{T_s}$ , and  $\langle i_{4_a} \rangle_{T_s}$ , plus control variables  $\langle v_d \rangle_{T_s}$  and  $\langle v_q \rangle_{T_s}$ .

Although the model is nonlinear, its variables reach constant values in steady state, making it valuable to analyze the behavior of the 4L-3P-NPC converter and to design proper control strategies.

#### 4.2. 4L-3P-DAB Converter Large-Signal Averaged Model

The derivation of the large-signal averaged model for the 4L-1P-DAB converter begins with establishing a phasor representation as the converter’s fundamental model, based on [20]. Figure 5 presents the sinusoidal steady-state model, focusing solely on the fundamental frequency, equated to the switching frequency  $f_s$  for simplicity [20,25]. This model considers two phase-shifted sinusoidal AC voltages with amplitudes determined by modulation angles  $\alpha_{x1}$ ,  $\alpha_{x2}$ , and  $\alpha_{x3}$ , where  $x \in \{a, b\}$ , as detailed below in Section 6.4.

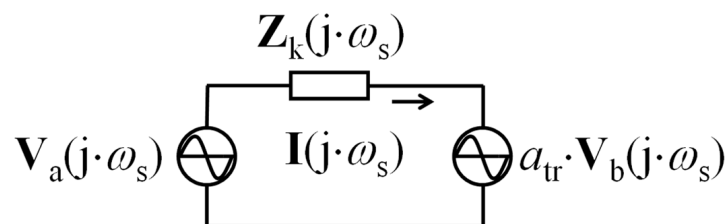


Figure 5. The fundamental model of the 4L-1P-DAB converter.

The key circuit parameters are defined as follows:

$$\left\{ \begin{array}{l} \mathbf{X}_{L_k}(j \cdot \omega_s) = \omega_s \cdot L_k \\ \mathbf{Z}_k(j \cdot \omega_s) = R_{L_k} + j \cdot \mathbf{X}_{L_k}(j \cdot \omega_s) \\ K_x = \frac{2}{3 \cdot \pi} \cdot (\cos(\frac{\pi}{2} - \alpha_{x1}) + \cos(\frac{\pi}{2} - \alpha_{x2}) + \cos(\frac{\pi}{2} - \alpha_{x3})), x \in \{a, b\} \\ \mathbf{V}_a(j \cdot \omega_s) = K_a \cdot v_{dca} \angle \theta_a \\ \mathbf{V}_b(j \cdot \omega_s) = a_{tr} \cdot K_b \cdot v_{dcb} \angle (\theta_a - \phi) \end{array} \right. \quad (11)$$

The AC voltage amplitudes are expressed as  $V_a(j \cdot \omega_s) = K_a \cdot v_{dca} \angle \theta_a$  and  $V_b(j \cdot \omega_s) = a_{tr} \cdot K_b \cdot v_{dcb} \angle (\theta_a - \phi)$ .

Power transfer at the HFT input  $P_{aHFT}$  and output  $P_{bHFT}$  is obtained and shown as follows:

$$\left\{ \begin{array}{l} P_{aHFT} = \mathcal{R}_e \{ \mathbf{V}_a(j \cdot \omega_s) \cdot \mathbf{I}^*(j \cdot \omega_s) \} \\ \mathbf{I}^*(j \cdot \omega_s) = \frac{1}{|\mathbf{Z}_k(j \cdot \omega_s)|} \cdot (K_a \cdot v_{dca} \cdot \sin(\theta_a + \sigma) - a_{tr} \cdot K_b \cdot v_{dcb} \cdot \sin(\theta_a - \phi + \sigma)) - \\ \quad - j \cdot \frac{1}{|\mathbf{Z}_k(j \cdot \omega_s)|} \cdot (K_a \cdot v_{dca} \cdot \sin(\theta_a - v) - a_{tr} \cdot K_b \cdot v_{dcb} \cdot \sin(\theta_a - \phi - v)) \\ \sigma = \tan^{-1} \left( \frac{R_{L_k}}{\mathbf{X}_{L_k}(j \cdot \omega_s)} \right), \quad v = \tan^{-1} \left( \frac{\mathbf{X}_{L_k}(j \cdot \omega_s)}{R_{L_k}} \right) \\ P_{aHFT} = \frac{K_a \cdot v_{dca}}{|\mathbf{Z}_k(j \cdot \omega_s)|} \cdot (K_a \cdot v_{dca} \cdot (\sin(\theta_a + \sigma) \cdot \cos \theta_a + \sin(\theta_a - v) \cdot \sin \theta_a) - \\ \quad - a_{tr} \cdot K_b \cdot v_{dcb} \cdot (\sin(\theta_a - \phi + \sigma) \cdot \cos \theta_a + \sin(\theta_a - \phi - v) \cdot \sin \theta_a)) \end{array} \right. \quad (12)$$

$$\left\{ \begin{array}{l} P_{bHFT} = -(P_{aHFT} + P_{R_{L_k}}) \\ P_{R_{L_k}} = R_{L_k} \cdot |\mathbf{I}(j \cdot \omega_s)|^2 \end{array} \right. \quad (13)$$

Considering  $\theta_a = 0$ , the maximum input power  $P_{aHFTmax}$  can be defined as follows:

$$P_{aHFT} = \frac{K_a \cdot V_{dca}}{|\mathbf{Z}_k(j \cdot \omega_s)|^2} \cdot (K_a \cdot R_{L_k} \cdot V_{dca} - a_{tr} \cdot K_b \cdot V_{dcb} \cdot |\mathbf{Z}_k(j \cdot \omega_s)| \cdot \sin(\varphi - \sigma)) \quad (14)$$

and the achieved phase shift  $\phi = \pi/2$  is aligned with the steady-state operation values in [20,25], confirming the validity of the model.

The dynamic large-signal model is obtained by developing the following:

$$\frac{d \langle v_{C_{a_k}} \rangle_{T_s}}{dt} = -\frac{1}{C_a} \cdot \left[ \frac{\langle v_{C_{a_k}} \rangle_{T_s}}{R_{C_a}} + \sum_{j \neq k} \frac{\langle v_{C_{a_j}} \rangle_{T_s} \cdot (\langle i_j \rangle_{T_s} + \langle i_{j_a} \rangle_{T_s})}{\sum_{m=1}^3 \langle v_{C_{a_m}} \rangle_{T_s}} + \frac{p_{dq} + p_{aHFT}}{\sum_{m=1}^3 \langle v_{C_{a_m}} \rangle_{T_s}} \right] \quad (15)$$

for  $\{j, k\} \in \{1, 2, 3\}$

$$\frac{d \langle v_{C_{b_k}} \rangle_{T_s}}{dt} = \frac{1}{C_b} \cdot \left[ -\frac{\langle v_{C_{b_k}} \rangle_{T_s}}{R_{C_b}} + \sum_{j \neq k} \frac{\langle v_{C_{b_j}} \rangle_{T_s} \cdot \langle i_{j_b} \rangle_{T_s}}{\sum_{m=1}^3 \langle v_{C_{b_m}} \rangle_{T_s}} + \frac{p_{aHFT} + p_{R_{L_k}}}{\sum_{m=1}^3 \langle v_{C_{b_m}} \rangle_{T_s}} - \langle i_{B_k} \rangle_{T_s} \right] \quad (16)$$

for  $\{j, k\} \in \{1, 2, 3\}$

These equations relate the AC grid in the D-Q frame with the a-side DC-link and also relate the HFT power terms  $p_{aHFT}$  and  $p_{bHFT}$  to the battery charging currents  $i_{B1}$ ,  $i_{B2}$ , and  $i_{B3}$ . This development provides an accurate representation of the large-signal behavior of the converter in steady-state and dynamic operation.

### 5. Small-Signal Model

The large-signal averaged models for the 4L-BC are established for the 4L-3P-NPC converter in (10) and for the 4L-1P-DAB converter in (15) and (16). Both models are

continuous but nonlinear. However, linear control techniques are preferred for simplicity and extensive experience.

To utilize linear control techniques, it is essential to linearize the large-signal averaged models by applying the perturbation technique and Taylor series development around the operating point of the system, as described in [32,34]. The operating points are calculated by setting the time derivatives to zero in (10), (15), and (16), and then substituting all variables with their steady-state expressions (denoted in capital letters). The resulting steady-state model of the 4L-BC is given by:

$$\left\{ \begin{aligned} & -R_{ac} \cdot I_d + \omega \cdot L_{ac} \cdot I_q - E_{lfl} + V_d = 0 \\ & -\omega \cdot L_{ac} \cdot I_d - R_{ac} \cdot I_q + V_q = 0 \\ & \frac{1}{R_{Ca}} \cdot V_{dca} + \frac{(-2 \cdot V_{Ca1} + V_{Ca2} + V_{Ca3})}{V_{dca}} \cdot (I_2 + I_{2a}) + \frac{(-V_{Ca1} - V_{Ca2} + 2 \cdot V_{Ca3})}{V_{dca}} \cdot (I_3 + I_{3a}) + 3 \cdot \frac{P_{dq} + P_{aHFT}}{V_{dca}} = 0 \\ & -\frac{1}{R_{Cb}} \cdot V_{dcb} + \frac{(-2 \cdot V_{Cb1} + V_{Cb2} + V_{Cb3})}{V_{dcb}} \cdot I_{2b} + \frac{(-V_{Cb1} - V_{Cb2} + 2 \cdot V_{Cb3})}{V_{dcb}} \cdot I_{3b} + 3 \cdot \frac{P_{aHFT} + P_{RLk}}{V_{dcb}} - (I_{B1} - I_{B2} - I_{B3}) = 0 \\ & -R_{dc} \cdot (I_{B1} + I_{B2} + I_{B3}) + V_{dcb} - (V_{B1} + V_{B2} + V_{B3}) = 0 \\ & P_{aHFT} = \frac{K_a \cdot V_{dca}}{|Z_k(j\omega_s)|^2} \cdot \{K_a \cdot R_{Lk} \cdot V_{dca} - a_{tr} \cdot K_b \cdot V_{dcb} \cdot |Z_k(j\omega_s)| \cdot \sin(\varphi - \sigma)\} \\ & P_{dq} = I_d \cdot V_d + I_q \cdot V_q \end{aligned} \right. \quad (17)$$

The model captures the dynamics of the voltage differences across capacitors  $C_a$  and  $C_b$  (denoted as  $v_{Cxy}$ , where  $x \in \{a, b\}$  and  $y \in \{1, 2, 3\}$ ), emphasizing the impact of the currents flowing through the midpoints (neutral points) on the capacitor voltage balance, which will be explored in a later subsection.

To simplify (17), known steady-state variables—including currents  $I_q, I_2, I_{2a}, I_3, I_{3a}, I_{2b}, I_{3b}, I_{B1}, I_{B2},$  and  $I_{B3}$  and voltages  $E_{lfl}, V_{Ca1}, V_{Ca2}, V_{Ca3}, V_{Cb1}, V_{Cb2}, V_{Cb3}, V_{B1}, V_{B2},$  and  $V_{B3}$ —are considered. Additionally, currents  $I_q$  and those flowing through the neutral points ( $I_2, I_{2a}, I_3, I_{3a}, I_{2b},$  and  $I_{3b}$ ) are assumed to be zero. This leads to obtaining the unknown variables  $I_d, V_d, V_q,$  and  $\phi$  defined by:

$$\left\{ \begin{aligned} I_d &= \sqrt{\left(\frac{E_{lfl}}{2 \cdot R_{ac}}\right)^2 - \frac{P_{aHFT}}{R_{ac}} - \frac{1}{3} \cdot \frac{V_{dca}^2}{R_{ac} \cdot R_{Ca}} - \frac{E_{lfl}}{2 \cdot R_{ac}}} \\ V_d &= E_{lfl} + R_{ac} \cdot I_d \\ V_q &= \omega \cdot L_{ac} \cdot I_d \\ \varphi &= \sin^{-1} \left\{ \frac{|Z_k(j\omega_s)| \cdot P_{aHFT}}{a_{tr} \cdot K_a \cdot K_b \cdot V_{dca} \cdot V_{dcb} \cdot X_{Lk}(j\omega_s)} - \frac{K_a \cdot R_{Lk} \cdot V_{dca}}{a_{tr} \cdot K_b \cdot V_{dcb} \cdot X_{Lk}(j\omega_s)} \right\} \end{aligned} \right. \quad (18)$$

From the steady-state variables defined in (18), the linearization process can be applied to obtain the small-signal model of the 4L-BC. The variables denoted with the symbol “^”, and the capital letters represent disturbances and steady-state operating points, respectively.

As a multivariable system, the linear model of the 4L-BC can be represented in state space form as follows:

$$\begin{cases} \dot{\mathbf{x}} = \mathbf{A} \cdot \mathbf{x} + \mathbf{B} \cdot \mathbf{u} \\ \mathbf{y} = \mathbf{C} \cdot \mathbf{x} + \mathbf{D} \cdot \mathbf{u} \end{cases} \quad (19)$$

where  $\mathbf{x}$  is the state vector,  $\mathbf{u}$  is the input vector, and  $\mathbf{y}$  is the output vector, defined as:

$$\begin{cases} \mathbf{x} = [\hat{i}_d, \hat{i}_q, \hat{v}_{Ca1}, \hat{v}_{Ca2}, \hat{v}_{Ca3}, \hat{v}_{Cb1}, \hat{v}_{Cb2}, \hat{v}_{Cb3}, \hat{i}_{B1}, \hat{i}_{B2}, \hat{i}_{B3}]^T \\ \mathbf{u} = [\hat{E}_{lfl}, \hat{v}_d, \hat{v}_q, \hat{v}_{B1}, \hat{v}_{B2}, \hat{v}_{B3}, \hat{i}_2, \hat{i}_{2a}, \hat{i}_3, \hat{i}_{3a}, \hat{i}_{2b}, \hat{i}_{3b}, \hat{\phi}]^T \end{cases} \quad (20)$$

$\mathbf{x} = \mathbf{y}$  where  $\{\mathbf{x}, \mathbf{y}\} \in \{\mathbb{R}^{11}\}$  and  $\mathbf{u} \in \{\mathbb{R}^{13}\}$

Regarding the assumption  $\mathbf{x} = \mathbf{y}$ , it should be noted that in a state space such (19),  $\mathbf{x}$  and  $\mathbf{y}$  are related but not necessarily equivalent. In fact,  $\mathbf{x}$  represents the state variables of the system, which describe the current state of the system. Instead, the output vector  $\mathbf{y}$  represents the measurable or observable variables of the system [34–36].

The state ( $\mathbf{A}$ ), input ( $\mathbf{B}$ ), output ( $\mathbf{C}$ ), and direct transmission ( $\mathbf{D}$ ) matrices are defined as follows:  $\mathbf{A} = \begin{bmatrix} \mathbf{A}_{11} & \mathbf{A}_{12} \\ \mathbf{A}_{21} & \mathbf{A}_{22} \end{bmatrix}$ ,  $\mathbf{B} = \begin{bmatrix} \mathbf{B}_{11} & \mathbf{B}_{12} \\ \mathbf{A}_{21} & \mathbf{A}_{22} \end{bmatrix}$ ,  $\mathbf{C} = \mathbf{I}$ , and  $\mathbf{D} = \mathbf{0}$ . Also, the submatrices  $\mathbf{A}_{jk}$  and  $\mathbf{B}_{jk}$ , where  $\{j, k\} \in \{1, 2\}$ , are defined in Appendix A. Symbolically,  $\{\mathbf{A}, \mathbf{C}\} \in \mathcal{M}_{11 \times 11}$  and  $\{\mathbf{B}, \mathbf{D}\} \in \mathcal{M}_{11 \times 13}$ . Moreover, the submatrices of  $\mathbf{A}$  can be defined as  $\mathbf{A}_{11} \in \mathcal{M}_{6 \times 6}$ ,  $\mathbf{A}_{12} \in \mathcal{M}_{6 \times 5}$ ,  $\mathbf{A}_{21} \in \mathcal{M}_{6 \times 6}$ , and  $\mathbf{A}_{22} \in \mathcal{M}_{6 \times 6}$ . The submatrices of  $\mathbf{B}$  can also be defined as  $\{\mathbf{B}_{11}, \mathbf{B}_{21}\} \in \mathcal{M}_{6 \times 6}$ ,  $\mathbf{B}_{12} \in \mathcal{M}_{6 \times 7}$ , and  $\mathbf{B}_{22} \in \mathcal{M}_{5 \times 7}$  (Appendix A). Finally,  $\mathbf{I}$  and  $\mathbf{0}$  are the identity and zero matrix, respectively.

Since the model presented in (19) is linear, and considering the aim of designing a control system for the 4L-BC using linear design techniques, the Laplace domain representation of the system model is obtained and shown as follows:

$$\left\{ \begin{array}{l} I_d(s) = \frac{1}{(s + K_1)} \cdot [K_2 \cdot I_q(s) - K_3 \cdot (E_{1H}(s) - V_d(s))] \\ I_q(s) = \frac{1}{(s + K_1)} \cdot [-K_2 \cdot I_d(s) + K_3 \cdot V_q(s)] \\ V_{C_{ai}}(s) = \frac{1}{(s + K_6)} \cdot \left[ -K_4 \cdot I_d(s) - K_5 \cdot I_q(s) + K_7 \cdot \sum_{j \neq i} V_{C_{aj}}(s) + K_8 \cdot V_{d_{cb}}(s) - K_9 \cdot V_d(s) + (-1)^i \cdot K_{10} \cdot (I_2(s) + I_{2a}(s)) + (-1)^{i+1} \cdot K_{11} \cdot (I_3(s) + I_{3a}(s)) - K_{12} \cdot \phi(s) \right] \\ \quad \text{for } \{i, j\} \in \{1, 2, 3\} \\ V_{C_{bi}}(s) = \frac{1}{(s + K_{16})} \cdot \left[ K_{15} \cdot V_{d_{ca}}(s) - K_{17} \cdot \sum_{j \neq i} V_{C_{bj}}(s) - K_{18} \cdot I_{B_i}(s) + (-1)^i \cdot K_{19} \cdot I_{2b}(s) + (-1)^{i+1} \cdot K_{20} \cdot I_{3b}(s) + K_{21} \cdot \phi(s) \right] \\ \quad \text{for } \{i, j\} \in \{1, 2, 3\} \\ I_{B_i}(s) = \frac{K_{24}}{(s + K_{25})} \cdot \{V_{C_{bi}}(s) - V_{B_i}(s)\} \\ \quad \text{for } i \in \{1, 2, 3\} \end{array} \right. \quad (21)$$

assuming zero initial conditions, as outlined in [34,37]. This representation in the Laplace domain facilitates the analysis and design of the control system in the frequency domain. The  $K$ -constants in (21) are defined in Appendix A.

### 6. Control System and Modulation Algorithms

The complete control system for the 4L-BC is illustrated in Figure 6, with key control objectives including battery charging current regulation, a-side DC-link voltage regulation (total and individual capacitor balance), and grid power factor control [23,24,38]. The 4L-3P-NPC converter controller is responsible for managing the total a-side DC-link voltage ( $v_{dca}$ ), controlling reactive power exchange with the grid (ensuring power factor correction), and balancing the a-side DC-link capacitor voltages ( $v_{Ca1}$ ,  $v_{Ca2}$ , and  $v_{Ca3}$ ) [27,28]. Meanwhile, the 4L-1P-DAB converter controller regulates the battery charging currents ( $i_{B1}$ ,  $i_{B2}$ , and  $i_{B3}$ ) and can also contribute to a-side DC-link capacitor voltage balancing [25,27]. This dual capability allows a-side DC-link voltage balancing to be achieved using the 4L-3P-NPC converter, the 4L-1P-DAB converter, or both simultaneously, as demonstrated in the three-level battery charger (3L-BC) [23,24]. This flexibility enables user customization based on specific performance and operational requirements.

The mathematical models describing the dynamic open-loop plants of the system are not covered exhaustively in this article. However, a detailed description of these models can be found in [38].

Modulation algorithms play a pivotal role in the operation of the proposed 4L-BC. For the 4L-3P-NPC converter, a virtual-vector pulsewidth modulation (VVPWM) strategy is employed, which enhances voltage balancing, reduces total harmonic distortion, and optimizes switching losses [28]. For the 4L-1P-DAB converter, a four-level extension of the modulation approach defined in [24] is utilized. This strategy involves dynamically adjusting the switching angles to create an optimized voltage waveform for both the primary and secondary sides of the HFT [25]. This modulation not only improves energy transfer efficiency but also ensures precise control over the charging currents of batteries with varying SoC.

By integrating these advanced modulation algorithms into the control architecture, the 4L-BC achieves superior performance in terms of efficiency, flexibility, and reliability.

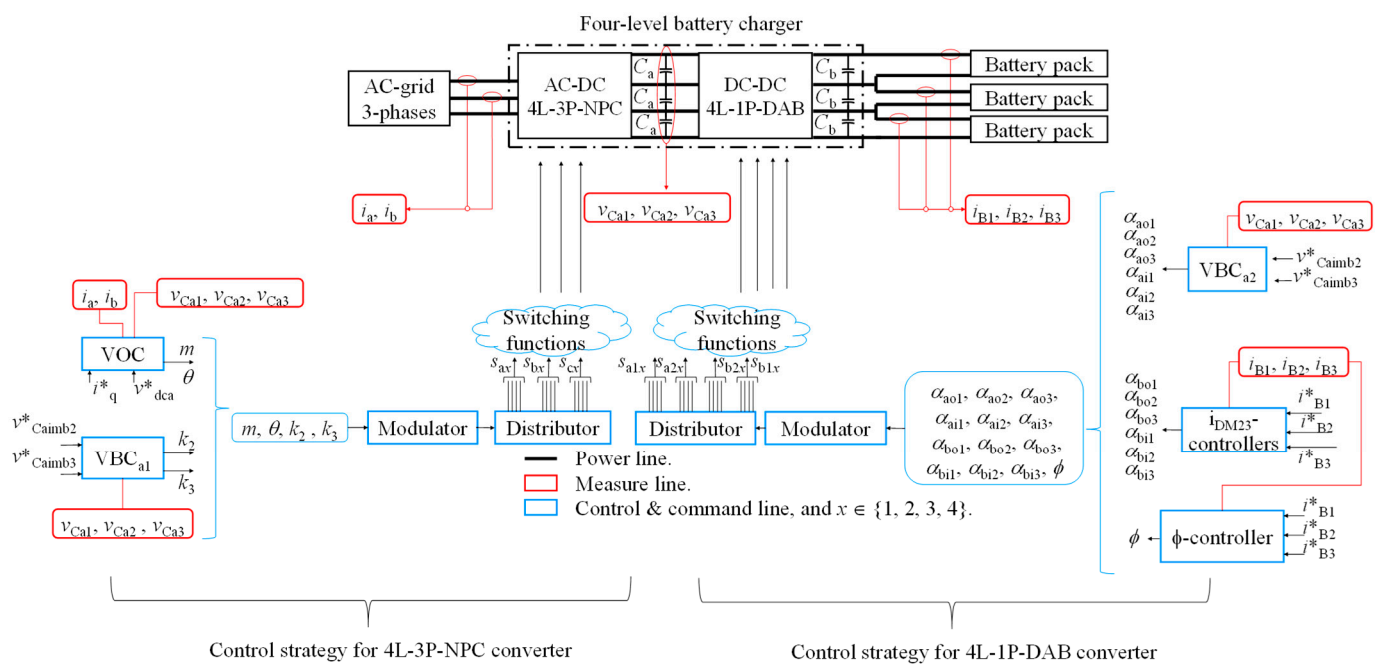


Figure 6. General battery charger control diagram.

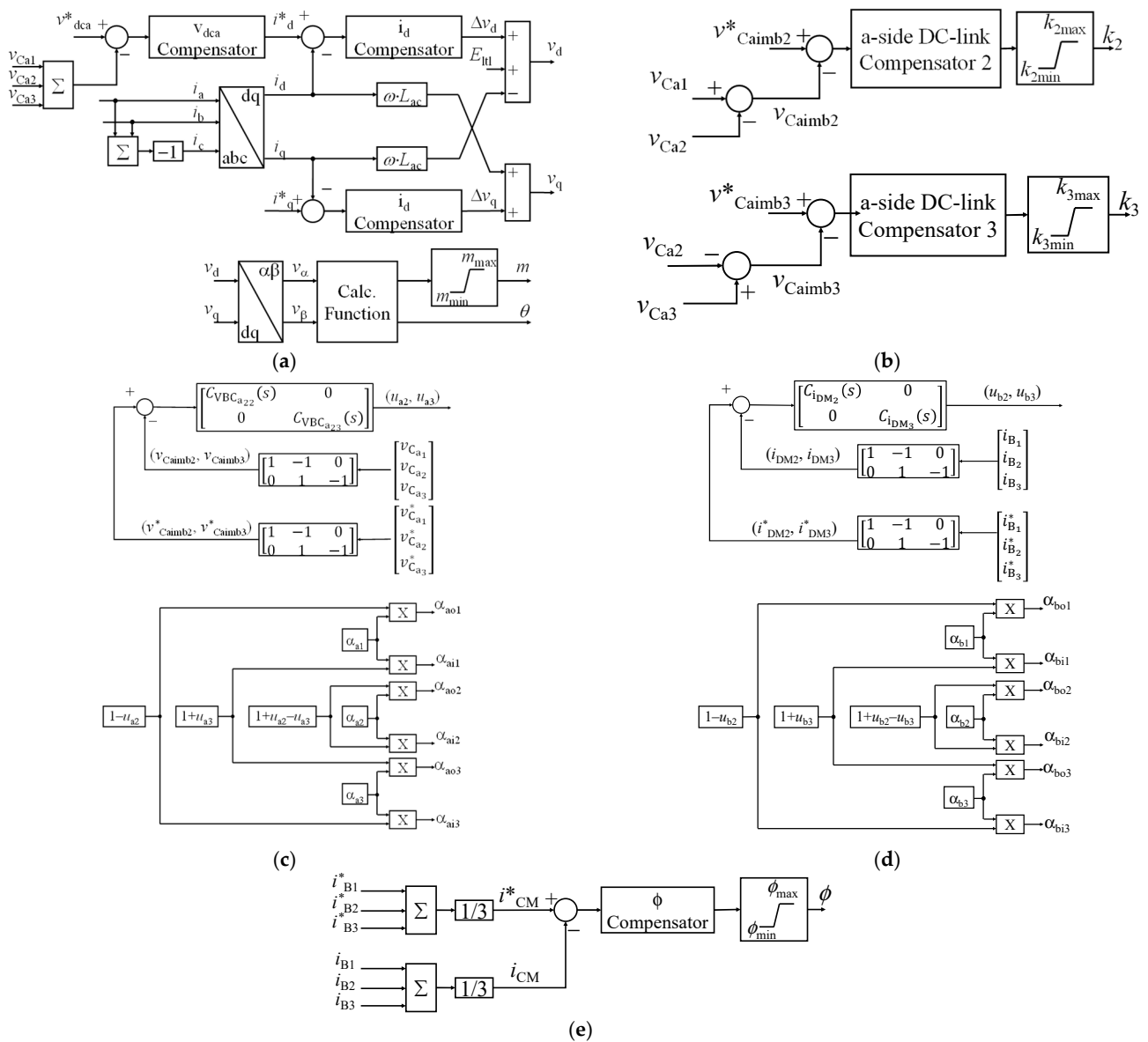
### 6.1. 4L-3P-NPC Converter Control Description

In this 4L-BC, the voltage-oriented control system is similar to the 3L-BC [23,24,38], but with an additional voltage level. The control system scheme is shown in Figure 7a.

The total a-side DC-link voltage ( $v_{dca}$ ) is regulated by a PI controller ( $v_{dca}$ -compensator), which provides the reference for the D-component of the grid current ( $i_d$ ) regulated by another PI controller ( $i_d$ -compensator). The Q-component of the grid current ( $i_q$ ) is regulated by a PI controller ( $i_q$ -compensator) to control the reactive power flow and maintain a unity power factor. The current controllers generate the  $v_d$  and  $v_q$  signals, which are then transformed into  $\alpha$ - $\beta$  variables to obtain the modulation index  $m = \sqrt{v_\alpha^2 + v_\beta^2}$  and the reference angle  $\theta = \text{atan}(v_\beta/v_\alpha)$  through a calculation function block (calc. function).

For a-side DC-link voltage balancing, the a-side DC-link compensator (VBC<sub>a1</sub>) is implemented (Figure 7b). Since the DC-link has three capacitors, there are two voltage unbalances to regulate,  $v_{Caimb2} = v_{Ca1} - v_{Ca2}$  and  $v_{Caimb3} = v_{Ca2} - v_{Ca3}$ . The implementation includes two compensators, a-side DC-link compensators 2 and 3, which generate control signals ( $k_2$  and  $k_3$ ) to reduce the unbalances to zero.

The control system consists of five compensators, namely the two current compensators ( $i_d$ ,  $i_q$ ), the a-side DC-link total voltage compensator ( $v_{dca}$ ), and the two voltage unbalance compensators ( $v_{Caimb2}$  and  $v_{Caimb3}$ ).



**Figure 7.** Control system diagrams. (a) Voltage-oriented controller for the 4L-3P-NPC converter (VOC). (b) A-side DC-link voltage balancing control of the 4L-3P-NPC converter (VBC<sub>a1</sub>) [27,28]. (c) A-side DC-link voltage balancing control of 4L-1P-DAB converter (VBC<sub>a2</sub>) [22,25]. (d) Regulation of the DM components of the battery pack currents ( $i_{DM2^-}$  and  $i_{DM2^+}$ -controller) [27]. (e) Control of the 4L-1P-DAB converter power transfer ( $\phi$  control) by regulating the CM component of the battery pack currents ( $i_{CM}$ ).

### 6.2. 4L-3P-NPC Converter Modulation

VVPWM is based on a set of space vectors in the space-vector diagram, called virtual vectors, which are defined as a linear combination of certain switching states [39]. Each virtual vector involves an average zero neutral-point current in every switching cycle. In this way, if the reference voltage vector is synthesized with these virtual vectors, the balance

of the voltages of the DC-link capacitors will be guaranteed in each switching cycle [26,40]. This modulation is suitable for this four-level converter and can be implemented as follows:

$$\begin{cases} mod_a(\theta) = \left(\frac{2}{\sqrt{3}}\right) \cdot m \cdot \cos(\theta) \\ mod_b(\theta) = \left(\frac{2}{\sqrt{3}}\right) \cdot m \cdot \cos\left(\theta - \frac{2 \cdot \pi}{3}\right) \\ mod_c(\theta) = \left(\frac{2}{\sqrt{3}}\right) \cdot m \cdot \cos\left(\theta + \frac{2 \cdot \pi}{3}\right) \end{cases} \quad (22)$$

$$\begin{cases} mod_{max}(\theta) = \max[mod_a, mod_b, mod_c] \\ mod_{min}(\theta) = \min[mod_a, mod_b, mod_c] \end{cases} \quad (23)$$

$$\begin{cases} d_{x_1}(\theta) = \frac{1}{2} \cdot (mod_{max} - mod_x) \\ d_{x_2}(\theta) = d_{x_3}(\theta) \\ d_{x_3}(\theta) = \frac{1}{2} \cdot (1 - d_{x_1}(\theta) - d_{x_4}(\theta)) \\ d_{x_4}(\theta) = \frac{1}{2} \cdot (d_{x_1}(\theta) - mod_{min}) \end{cases} \quad (24)$$

$$\begin{aligned} m' &= \frac{m}{1+k_2 \cdot \frac{v_{Ca_3}+v_{Ca_2}-v_{Ca_1}}{v_{dca}} + k_3 \cdot \frac{v_{Ca_3}-v_{Ca_2}-v_{Ca_1}}{v_{dca}}} \\ \Rightarrow r &= \frac{m'}{m} = \frac{1}{1+k_2 \cdot \frac{v_{Ca_3}+v_{Ca_2}-v_{Ca_1}}{v_{dca}} + k_3 \cdot \frac{v_{Ca_3}-v_{Ca_2}-v_{Ca_1}}{v_{dca}}} \end{aligned} \quad (25)$$

$$\begin{cases} d'_{x_1}(\theta) = d_{x_1} \cdot (1 - k_2 - k_3) \cdot r \\ d'_{x_2}(\theta) = d_{x_2} \cdot + k_2 \cdot (d_{x_1} - d_{x_4}) \\ d'_{x_3}(\theta) = d_{x_3} \cdot + k_3 \cdot (d_{x_1} - d_{x_4}) \\ d'_{x_4}(\theta) = d_{x_4} \cdot (1 + k_2 + k_3) \cdot r \end{cases} \quad (26)$$

where  $x \in \{a, b, c\}$  [28].

In (24), the basic form of the leg duty ratios is calculated, without considering the control action determined by the closed-loop capacitor voltage balancing control. While the modulation strategy aims to achieve capacitor voltage balance in all operating conditions, non-idealities in the converter can still cause slight capacitor voltage unbalance.

Therefore, the closed-loop capacitor voltage balance control shown in Figure 7b becomes necessary. The closed-loop control in Figure 7b generates control parameters  $k_2$  and  $k_3$ , which modify the values of the open-loop leg duty cycles given in (26). This modification is required to ensure proper capacitor voltage balancing in the presence of converter non-idealities.

The correction factor  $r$  defined in (25) is necessary to prevent the capacitor voltage balancing action from perturbing the intended  $m$  value when the DC-link capacitor voltages are different. It ensures that the voltage balancing control does not affect the desired  $m$ , maintaining converter performance and stability.

### 6.3. 4L-1P-DAB Converter Control Description

The control schemes for the 4L-1P-DAB are shown in Figure 7c–e [25,27]. The 4L-1P-DAB converter has the capability to regulate the imbalance of the voltages  $v_{Ca_1}$ ,  $v_{Ca_2}$ , and  $v_{Ca_3}$  (VBC<sub>a2</sub>) similar to the 3L-3P-NPC converter (VBC<sub>a1</sub>) [23,24,38]. The control efforts  $u_{a2}$  and  $u_{a3}$  are produced to achieve a zero imbalance, i.e.,  $v_{Caimb2} = v_{Ca_1} - v_{Ca_2}$  and  $v_{Caimb3} = v_{Ca_2} - v_{Ca_3}$ , controlling the necessary switching angles  $\alpha_{axy}$  where  $x \in \{o, i\}$  and  $y \in \{1, 2, 3\}$  [25].

In addition, the 4L-1P-DAB converter regulates the battery pack charging currents  $i_{B1}$ ,  $i_{B2}$ , and  $i_{B3}$  by controlling the differential-mode (DM) and common-mode (CM) components, i.e.,  $i_{DM2} = i_{B1} - i_{B2}$ ,  $i_{DM3} = i_{B2} - i_{B3}$ , and  $i_{CM} = (i_{B1} + i_{B2} + i_{B3})/3$  [27]. The control efforts

$u_{b2}$  and  $u_{b3}$  produce the necessary switching angles  $\alpha_{bxy}$ , where  $x \in \{o, i\}$  and  $y \in \{1, 2, 3\}$ , for the proper operation of the modulator of the 4L-1P-DAB converter (Figure 7d).

Figure 7e shows the control diagram for  $i_{CM}$  control, where the power transfer of the 4L-1P-DAB converter is regulated by controlling the phase angle  $\phi$  [27].

The control system associated with the 4L-1P-DAB converter is constituted by five PI compensators, the detailed development of which can be found in [38].

#### 6.4. 4L-1P-DAB Converter Modulation

The switching strategy for this four-level converter, as shown in Figure 8, is based on modifying the switching angles to achieve a specific shape of the voltages on the primary and secondary sides of the HFT [25]. Figure 8 illustrates the waveforms of the voltages on the primary ( $v_{aT}$ ) and secondary ( $v_{bT}$ ) sides of the HFT, the voltage across inductance  $L_k$  ( $v_{Lk}$ ), and the current flowing through the a-side of the HFT ( $i_{aT}$ ). Moreover, this modulation strategy aims to build seven levels in the voltages  $v_{aT}$  and  $v_{bT}$ . The power transfer between the a- and b-side of the converter is regulated through the phase-shift angle  $\phi$  and the switching angles  $\alpha_{zjk}$ , where  $z \in \{a, b\}$ ,  $j \in \{i, o\}$ , and  $k \in \{1, 2, 3\}$ .

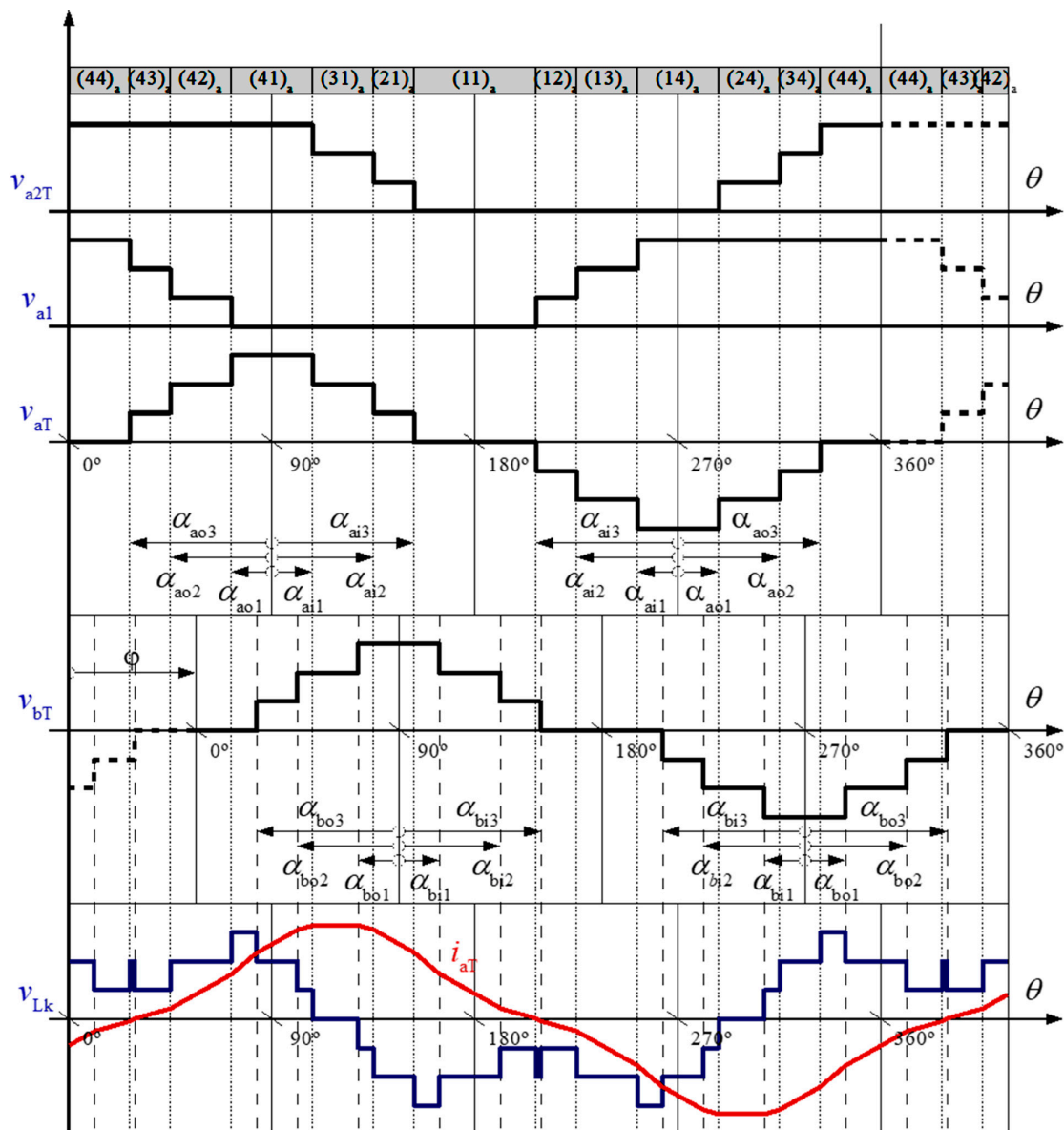


Figure 8. Voltage waveform  $v_{aT}$ ,  $v_{bT}$ ,  $v_{Lk}$ , and  $i_{aT}$  for the switching strategy in [25].

It is worth mentioning that for  $z \in \{a, b\}$ ,  $v_{zT}$  exhibits a predetermined switching state sequence as depicted in the top Figure 8.

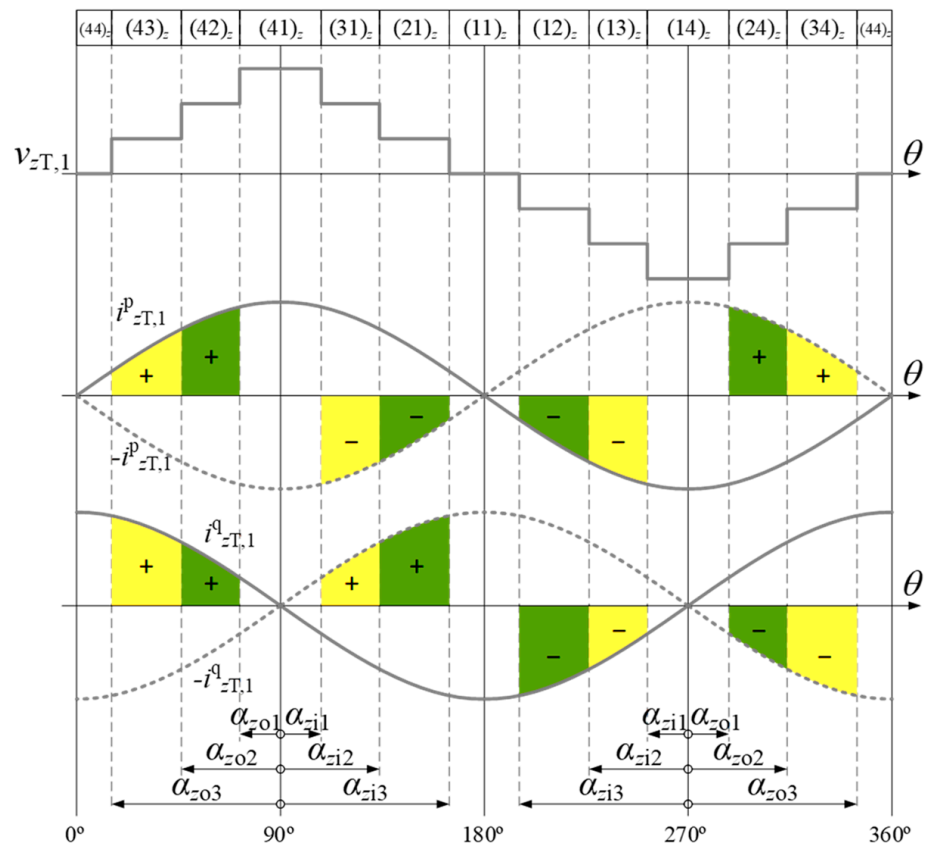
The six switching angles per side ( $\alpha_{zi1}$ ,  $\alpha_{zi2}$ ,  $\alpha_{zi3}$ ,  $\alpha_{zo1}$ ,  $\alpha_{zo2}$ , and  $\alpha_{zo3}$ ) plus the  $\phi$  sum up 13 degrees-of-freedom available to control capacitor voltage balancing, converter performance, and power flow. If  $\alpha_{z1} = \alpha_{zo1} = \alpha_{zi1z}$ ,  $\alpha_{z2} = \alpha_{zo2} = \alpha_{zi2z}$ , and  $\alpha_{z3} = \alpha_{zo3} = \alpha_{zi3z}$ , and the DC-link capacitor voltages are balanced, then quarter-wave symmetry is guaranteed and even order harmonics are eliminated in  $v_{aT}$ ,  $v_{bT}$ ,  $v_{Lk}$ , and  $i_{aT}$  waveforms [25].

The operating principle of this modulation involves drawing or injecting current from the two neutral points of the a- and b-side DC-link ( $i_{2z}$  and  $i_{3z}$ , where  $z \in \{a, b\}$ ) to balance the voltages  $v_{Cax}$  and  $v_{Cbx}$ , where  $x \in \{1, 2, 3\}$ . That is,  $v_{Ca1} = v_{Ca2} = v_{Ca3}$  and  $v_{Cb1} = v_{Cb2} = v_{Cb3}$  [25]. The currents  $i_{2z}$  and  $i_{3z}$  are defined as follows:

$$\begin{cases} i_{2z} = -(s_{2_z z_{1T}} - s_{2_z z_{2T}}) \cdot i_{zT} \\ i_{3z} = -(s_{3_z z_{1T}} - s_{3_z z_{2T}}) \cdot i_{zT} \end{cases} \quad (27)$$

based on the switching model of the 4L-1P-DAB converter, i.e., Equation (4).

To maintain the balance of the a- and b-side DC-link voltages, the total charge injected into the neutral points in a switching cycle must be zero [25]. To simplify the analysis, it is convenient to consider only the fundamental component of  $i_{zT}$ , i.e.,  $i_{zT,1}$ , as its amplitude is larger than the harmonic amplitudes and is the main contributor to  $i_{2z}$  and  $i_{3z}$ . Moreover, as shown in Figure 9,  $i_{zT,1}$  can be decomposed into the in-phase and in-quadrature components with respect to  $v_{zT,1}$  (the fundamental component of  $v_{zT}$ , where  $z \in \{a, b\}$ ).



**Figure 9.** Voltage  $v_{zT,1}$  and the in-phase and in-quadrature components of  $i_{zT}$  fundamental component ( $i^p_{zT,1}$ ;  $i^q_{zT,1}$ ). The green and yellow areas depict the injected (+) or drawn (−) charge from the z-side DC-link neutral points  $2_z$  and  $3_z$ , respectively, by  $i^p_{zT,1}$ ; and  $i^q_{zT,1}$  [25].

To study the dynamics of the charge injection at the neutral points, the effects of the fundamental component of  $i_{zT}$ , denoted as  $i_{zT,1}$ , are explored. As its amplitude is larger than the harmonic amplitudes, the effect of the harmonics on the capacitor voltages can be neglected. According to [22,25] and Figures 6 and 7,  $i_{zT,1}$  can be decoupled into a component in phase and a component in quadrature with  $v_{zT,1}$  (fundamental component of  $v_{zT}$ ), as mentioned before, denoted as  $i_{zT,1}^p$  and  $i_{zT,1}^q$ , respectively. The voltage and current  $v_{zT,1}$  and  $i_{zT,1}$  are defined by [22,25]:

$$\begin{cases} v_{zT,1} = V_{zT,1} \cdot \sin(\theta) \\ i_{zT,1} = i_{zT,1}^p + i_{zT,1}^q = I_{zT,1}^p \cdot \sin(\theta) + I_{zT,1}^q \cdot \cos(\theta) \end{cases} \quad (28)$$

Also, Figure 9 plots the voltage  $v_{zT}$  and the currents  $i_{zT,1}^p$  and  $i_{zT,1}^q$  as a function of  $\theta_z$  (the phase angle of  $v_{zT,1}$ ). The green- and yellow-shaded areas represent the electric charges injected toward (positive sign) and drawn from (negative sign) the DC-link neutral points  $2_z$  and  $3_z$ , respectively. These charges are provided by the currents  $i_{zT,1}^p$  and  $i_{zT,1}^q$ . To keep a preexisting capacitor voltage balance, the sum of the yellow areas must be zero and the sum of the green areas must also be zero. This is accomplished if the following is satisfied:

$$\sin(\alpha_{z1}) + \sin(\alpha_{z3}) - 2 \cdot \sin(\alpha_{z2}) = 0 \quad (29)$$

However, even when (29) is satisfied, converter non-idealities may lead to non-zero average neutral-point currents causing capacitor voltage unbalances. Any voltage imbalance in  $v_{Cax}$  and  $v_{Cbx}$ , where  $x \in \{1, 2, 3\}$ , can be corrected by modifying switching angles  $\alpha_{zjk}$  (where  $z \in \{a, b\}$ ,  $j \in \{i, o\}$ , and  $k \in \{1, 2, 3\}$ ) in order to inject or draw charge within a switching period. Note that this electric charge is only supplied by  $i_{z\_HFT,1}^p$ , since the total charge injected by  $i_{z\_HFT,1}^q$  is zero due to the odd symmetry of  $v_{zT}$  [25,40].

### 6.5. Control System Transfer Function

The system modeling is described in Sections 3–5. This modeling procedure resulted in the linear Equation (21) that describes the behavior of the system. Considering model (21) and the control system schemes described in the previous subsections, the control system transfer functions (TFs) that characterize the dynamics of the closed-loop system can be obtained. This section provides a theoretical analysis of these TFs.

As previously introduced, the 4L-BC is composed of a cascaded configuration integrating a 4L-3P-NPC and a 4L-1P-DAB. Each converter operates under a dedicated multiloop control framework designed to meet specific objectives such as DC-link voltage regulation, grid current tracking, voltage balancing, and controlled power flow. It is worth noting that the averaged and linearized models of the system obtained from the modeling procedure were used to tune the controllers. The explicit mathematical expressions of the TFs are detailed in Appendix A, and the controller design methodology used in this work is described in [38].

#### 6.5.1. Voltage Regulation Loop—4L-3P-NPC

The outer voltage regulation loop of the 4L-3P-NPC converter governs the total a-side DC-link voltage, denoted as  $v_{dca}$ . The associated transfer function, representing the plant to be controlled, is given by:

$$G_{v_{dca}}(s) = \left. \frac{V_{dca}(s)}{I_d(s)} \right|_{Y(s)=0} \quad (30)$$

This TF (see Appendix A) describes the interactions between the AC-side grid current  $I_d$ , the DC-link capacitors  $C_a$ , resistive losses  $R_{Ca}$ , and the interconnection impedance  $|Z_k(j\omega_s)|$  influenced by the DAB stage. It results in a high-order coupled system that includes both fast-switching and low-frequency dynamics. The pole-zero distribution of this TF is nontrivial, featuring multiple dominant poles associated with energy storage elements and parasitic resistances. This complexity requires careful controller design to achieve stability and bandwidth objectives.

#### 6.5.2. DQ-Frame Current Regulation Loops

The inner loops of the 4L-3P-NPC converter regulate the d- and q-axis components of the grid current. These currents are crucial for enforcing grid-side power factor correction and establishing reference-tracking behavior. Both axes are governed by a shared second-order plant model, expressed as:

$$G_d(s) = G_q(s) = G_{dq}(s) = \frac{I_d(s)}{V_d(s)} = \frac{I_q(s)}{V_q(s)} \quad (31)$$

(refer to Appendix A). This TF encapsulates the behavior of the LC filter and its interaction with the grid impedance. The zero at  $s = -\xi \cdot \omega_n$  enhances phase response, allowing for higher control bandwidth while maintaining a sufficiently large phase margin. The pole placement is linked to the natural frequency  $\omega_n$  and damping ratio  $\xi$ , both of which are functions of  $R_{ac}$  and  $L_{ac}$ . These loops serve as the backbone for the voltage control loop, providing a fast dynamic response necessary to maintain tight regulation under transient disturbances.

#### 6.5.3. A-Side DC-Link Voltage Balancing

The three a-side DC-link capacitors may exhibit voltage imbalances due to asymmetries in load or converter operation. Two dedicated loops are implemented to actively balance the voltages by controlling the imbalance terms:

$$\begin{cases} v_{C_{a_{imb2}}} = v_{C_{a1}} - 0.5 \cdot (v_{C_{a2}} + v_{C_{a3}}) \\ v_{C_{a_{imb3}}} = 0.5 \cdot (v_{C_{a1}} + v_{C_{a2}}) - v_{C_{a3}} \end{cases} \quad (32)$$

The corresponding plant dynamics are governed by first-order TFs:

$$G_{C_{a_{imbk}}}(s) = \frac{V_{C_{a_{imbk}}}(s)}{I_k(s)} \quad (33)$$

where  $k \in \{2, 3\}$  (see Appendix A). These functions reflect the RC-like dynamics of charge balancing among the capacitor banks. Dominant poles are determined by the product  $R_{Ca} \cdot C_a$ , and the system is inherently stable. However, due to their low-pass nature, these loops must be carefully compensated to prevent slow behavior or excessive control action during large transients [41].

#### 6.5.4. Differential-Mode Current Control—4L-1P-DAB

The DM current control loops are designed to regulate the charging current imbalance across the individual battery packs. These loops act on the differential currents:

$$\begin{cases} i_{DM2} = i_{B1} - i_{B2} \\ i_{DM3} = i_{B2} - i_{B3} \end{cases} \quad (34)$$

The associated plant TFs are modeled as second-order systems:

$$G_{C_{imb_k}}(s) = \frac{I_{DM_k}(s)}{I_{k_b}(s)} \quad (35)$$

where  $k \in \{2, 3\}$  (see Appendix A). These TFs include poles determined by the coupled dynamics of the DAB converter modulation index, interlink inductance  $L_k$ , and battery pack voltages. Resonant behavior may arise depending on pole locations, and loop gain compensation must account for potential peaking in frequency response.

#### 6.5.5. Common-Mode Current Control and Power Transfer

The net power transfer from the AC-side grid to the battery bank is controlled through the regulation of the common-mode current component defined by:

$$i_{CM} = \frac{1}{3} \cdot \sum_{j=1}^3 i_{B_j} \quad (36)$$

The plant TF associated with this loop is modeled as shown as follows:

$$G_{\phi}(s) = \frac{I_{CM}(s)}{\phi(s)} \quad (37)$$

which is defined in Appendix A.

The presence of a right-half-plane zero at  $s = -\omega_z$  introduces a non-minimum phase characteristic, imposing a theoretical upper limit on control bandwidth. The cubic denominator includes dominant low-frequency poles resulting from interactions between converter inductance, DC-link dynamics, and modulation phase angle  $\phi$ . The sensitivity of this loop to parameter variations and input disturbances requires conservative tuning strategies, especially in systems where rapid power fluctuations may occur.

## 7. Simulation Results

### 7.1. Specifications, Scenarios, and Cases Definition

Simulations were carried out with the model shown in Figure 1, using MATLAB/Simulink, version R2019b. The 4L-BC was connected to a three-phase AC grid with  $E_{l_{ll\_ss}} = 400$  Vrms line-to-line and  $f = 50$  Hz. Both converters in the 4L-BC operated with a switching frequency  $f_s = 10$  kHz.

The converter parameter values are listed in Table 1. The initial a-side DC-link capacitor voltages are  $v_{Ca10} = 280$  V,  $v_{Ca20} = 420$  V, and  $v_{Ca30} = 700$  V; i.e., the system starts with the a-side DC-link with its voltages imbalanced. The a-side DC-link voltage reference is set at  $v_{dca}^* = 1.4$  kV. The initial voltages of the b-side DC-link capacitors  $v_{Cb10}$ ,  $v_{Cb20}$ , and  $v_{Cb30}$  are imposed by the voltages of each battery pack  $v_{B1}$ ,  $v_{B2}$ , and  $v_{B3}$ . Charging current references  $i_{B1}^*$ ,  $i_{B2}^*$ , and  $i_{B3}^*$  are set to 100 A. The switching angles are initially defined as follows:  $\alpha_{z1} = 10^\circ$ ,  $\alpha_{z2} = 35.4^\circ$ , and  $\alpha_{z3} = 80^\circ$ , where  $z \in \{a, b\}$ , which are consistent with (29) and thus force  $i_{P_{zT,1}}$  to deliver a zero charge to the inner DC-link points [22,25].

Four different scenarios are generated for this 4L-BC according to four different capacitance ratings of the a-side DC-link capacitors, as shown in Table 2.

Similarly to the analysis for the 3L-BC case performed in [24], the characteristics and performance under each scenario are studied in the same three cases that were defined in the 3L-BC. As shown in Table 3, these cases are defined depending on the converters in charge of balancing the a-side DC-link, that is, to keep  $v_{Ca1}$ ,  $v_{Ca2}$ , and  $v_{Ca3}$  balanced.

**Table 1.** Converter parameters values [24].

Parameters	Values
$R_{ac}$	10 [mΩ]
$L_{ac}$	1 [mH]
$R_{Ca} = R_{Cb}$	10 [kΩ]
$C_b$	800 [μF]
$L_k$	25 [μH]
$L_m$	10 [H]
$R_{Lk}$	50 [mΩ]
$a_{tr}$	1
$R_{dc}$	20 [mΩ]
$L_{dc}$	1 [mH]
$f$	50 [Hz]
$f_s$	10 [kHz]

**Table 2.** Definition of studied scenarios depending on the a-side DC-link capacitor value  $C_a$ .

Parameter	Scenario 1	Scenario 2	Scenario 3	Scenario 4
$C_a$	300 [μF]	600 [μF]	800 [μF]	1100 [μF]

**Table 3.** Definition of studied cases depending on the converter in charge of balancing the a-side DC-link.

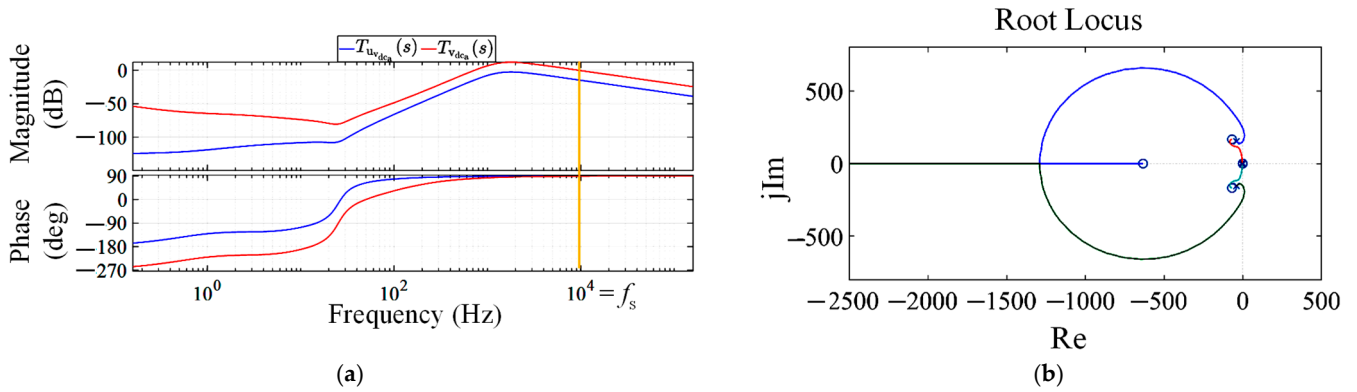
Case	Converter
1	only 4L-3P-NPC
2	only 4L-1P-DAB
3	both 4L-3P-NPC and 4L-1P-DAB

## 7.2. System Stability Analysis

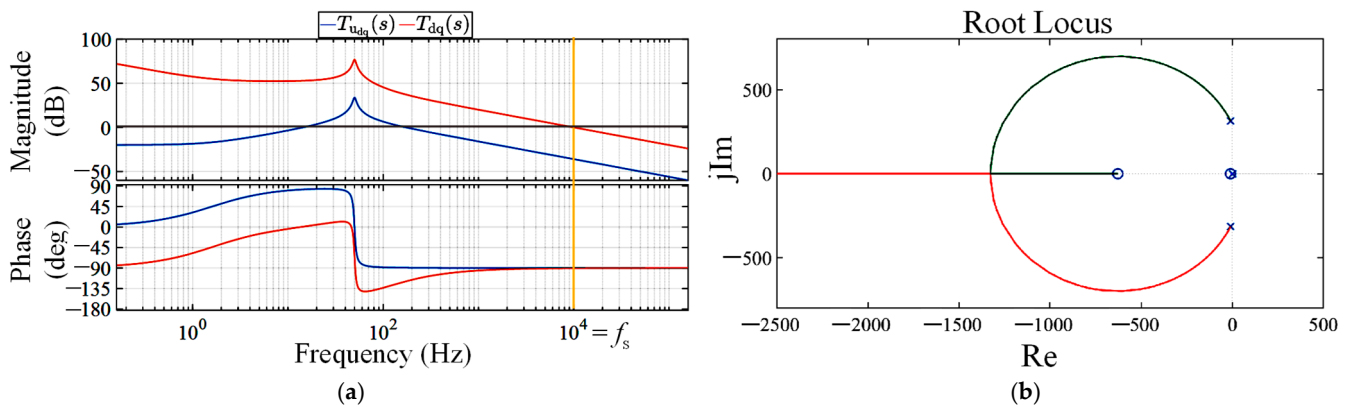
As detailed in previous sections, the linear model of the system was used to tune the controllers described in Section 6, as documented in [38]. A detailed frequency-domain stability analysis was carried out for all closed-loop systems in the 4L-BC architecture. Each control loop—covering DC-link voltage, DQ-frame current, voltage balancing, DM, and CM components—was subjected to classical loop-gain analysis using Bode plot evaluation and root locus inspection. As described in [38], the crossover frequency of each compensated open-loop transfer function was tuned to match the converter switching frequency  $f_s = 10$  kHz, ensuring minimal phase lag, high disturbance rejection, and fast transient response.

Figure 10a shows that the uncompensated open-loop gain  $T_{vdcau}(s)$  of the 4L-3P-NPC converter outer voltage loop lacks a crossover near  $f_s$ . However, after compensator insertion, the resulting loop gain  $T_{vdca}(s)$  exhibits a crossover precisely at  $f_s$  with a substantial phase margin of  $270^\circ$ , confirming stability and responsiveness. The corresponding root locus diagram in Figure 10b reveals all poles confined to the left-half complex plane, further validating system stability.

Similarly, the DQ-frame current controllers—governing  $G_{dq}(s)$ —show uncompensated crossover points at 30 Hz and 102 Hz (Figure 11a, blue). After compensation, the gain crossover shifts toward  $f_s$ , with a phase margin of  $86^\circ$  (Figure 11a, red). The root locus plot in Figure 11b confirms left-half-plane pole placement, affirming robust current control.

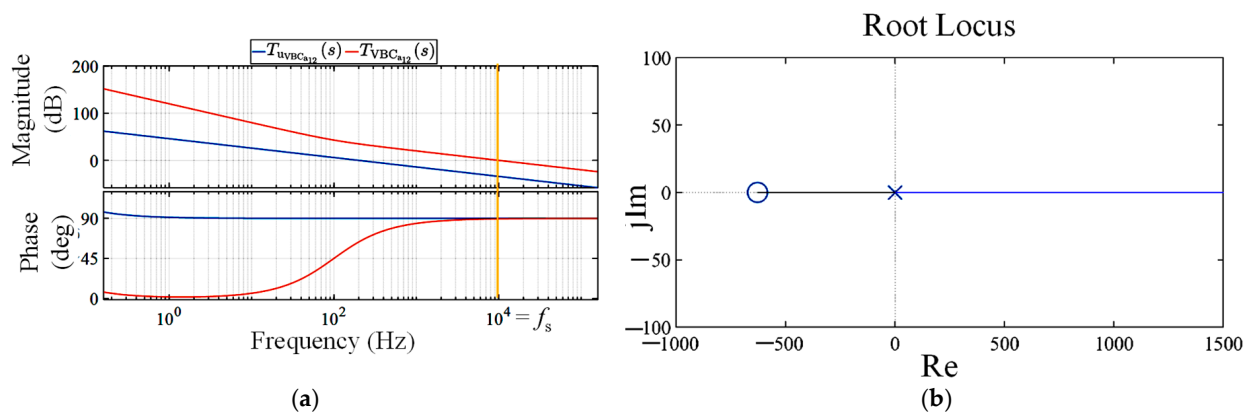


**Figure 10.** Bode plot and root locus diagram of the closed loop described in Figure 7a [38]. (a) Bode plot of  $T_{vdcau}(s)$  (blue color) and  $T_{vdca}(s)$  (red color). The orange line indicates the  $f_s$ . (b) Root locus diagram of  $T_{vdca}(s)$ . Green curves originate from real-axis poles, blue curves from complex poles with circular paths, and red segments highlight underdamped.



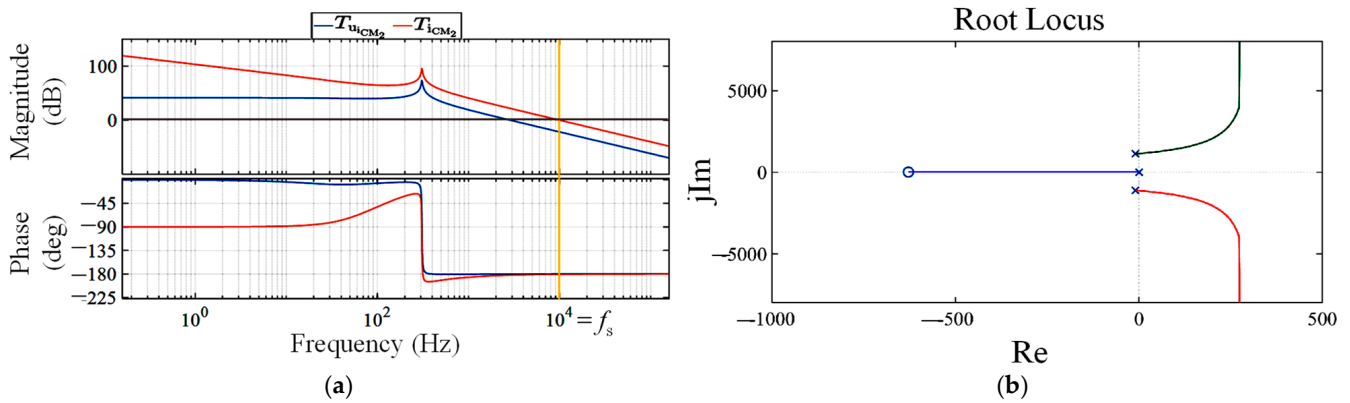
**Figure 11.** Bode plot and root locus diagram of the closed loop described in Figure 7a [38]. (a) Bode plot of  $T_{dqu}(s)$  (blue color) and  $T_{dq}(s)$  (red color). The orange line indicates the  $f_s$ . (b) Root locus diagram of  $T_{dq}(s)$ . Red curves denote low-damping regions, green indicate stable movement.

The voltage balancing loops  $C_{VBCa12}(s)$  and  $C_{VBCa13}(s)$ , governing imbalances  $v_{Caimb2}$  and  $v_{Caimb3}$ , also exhibit crossover frequencies at  $f_s$  with phase margins exceeding  $270^\circ$ , as seen in Figure 12a,b. This implies the excellent dynamic suppression of capacitor voltage

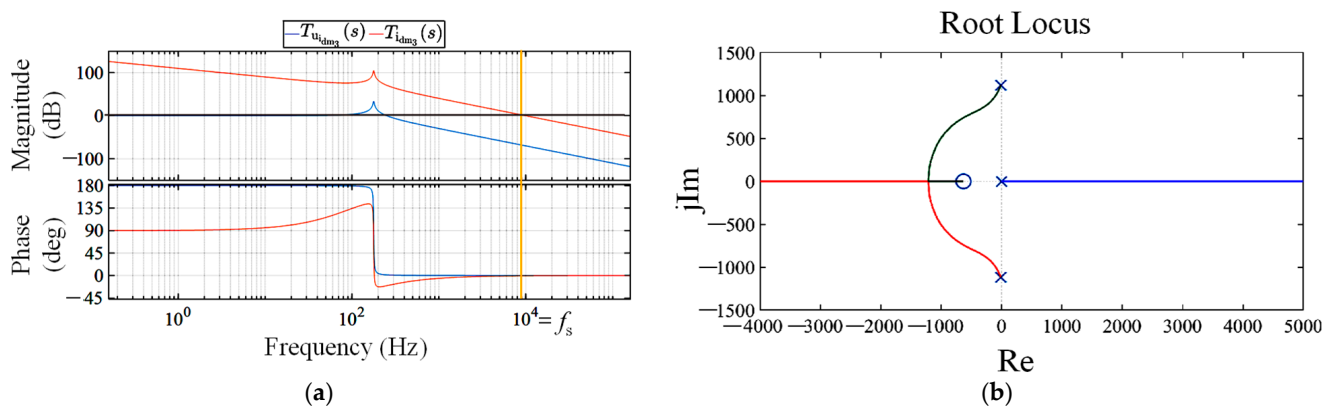


**Figure 12.** Bode plot and root locus diagram of the closed loop described in Figure 7b. (a) Bode plot of  $T_{VBCa12u}(s)$  (blue color) and  $T_{VBCa12}(s)$  (red color). The orange line indicates the  $f_s$ . (b) Root locus diagram of  $T_{VBCa12}(s)$ . Blue and green curves represent stable trajectories mismatch across varying load and voltage conditions.

On the 4L-1P-DAB side, Figures 13 and 14 reveal that the DM current controllers,  $T_{iDM2}(s)$  and  $T_{iDM3}(s)$ , are very stable, exceeding  $360^\circ$  of phase margin. This high phase margin is attributed to the inherent second-order plant dynamics and well-tuned compensators.



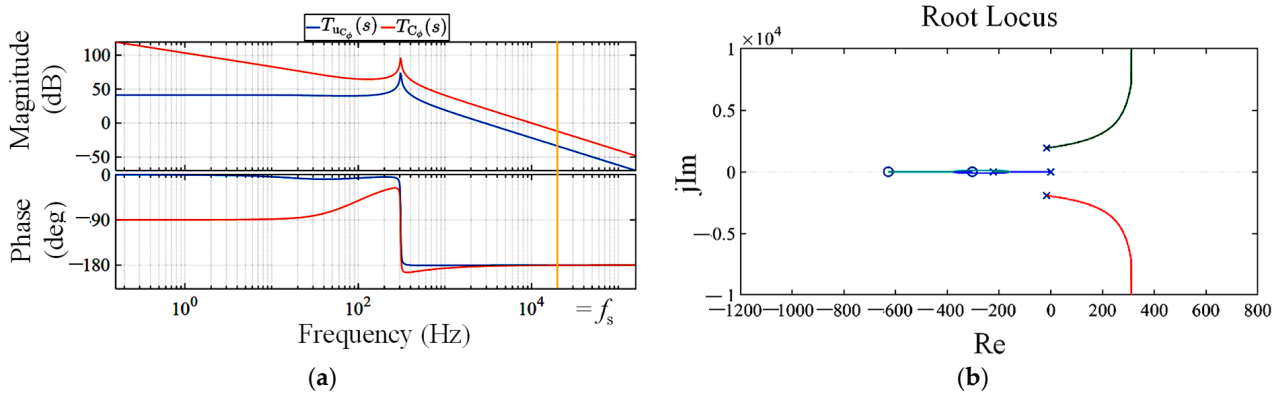
**Figure 13.** Bode plot and root locus diagram of the closed loop described in Figure 7d. (a) Bode plot of  $T_{iDM2u}(s)$  (blue color) and  $T_{iDM2}(s)$  (red color) The orange line indicates the  $f_s$ . (b) Root locus diagram of  $T_{iDM2}(s)$ . Blue shows real-axis path; red and green show complex conjugate branches as gain increases, illustrating dynamic response and stability trends.



**Figure 14.** Bode plot and root locus diagram of the closed loop described in Figure 7d. (a) Bode plot of  $T_{iDM3u}(s)$  (blue color) and  $T_{iDM3}(s)$  (red color) The orange line indicates the  $f_s$ . (b) Root locus diagram of  $T_{iDM3}(s)$ . The blue curve shows the real-axis pole migration, while red and green indicate divergent and stable complex branches as gain increases.

Finally, the most demanding control loop—the common-mode current controller regulating  $i_{CM}$  through phase angle  $\phi$ —is analyzed in Figure 15. Despite the non-minimum phase behavior of  $G_\phi(s)$ , the compensated loop  $T_\phi(s)$  achieves a robust phase margin of  $258^\circ$ , with root locus analysis verifying strict left-half-plane pole locations.

In conclusion, all control loops within the 4L-BC system—whether linear or nonlinear, single-input or multiple-input multiple-output—are well compensated, phase-stable, and dynamically resilient. These results validate the theoretical modeling presented in Section 6.5 and demonstrate the practical effectiveness of the control architecture under both steady-state and dynamic operating conditions.

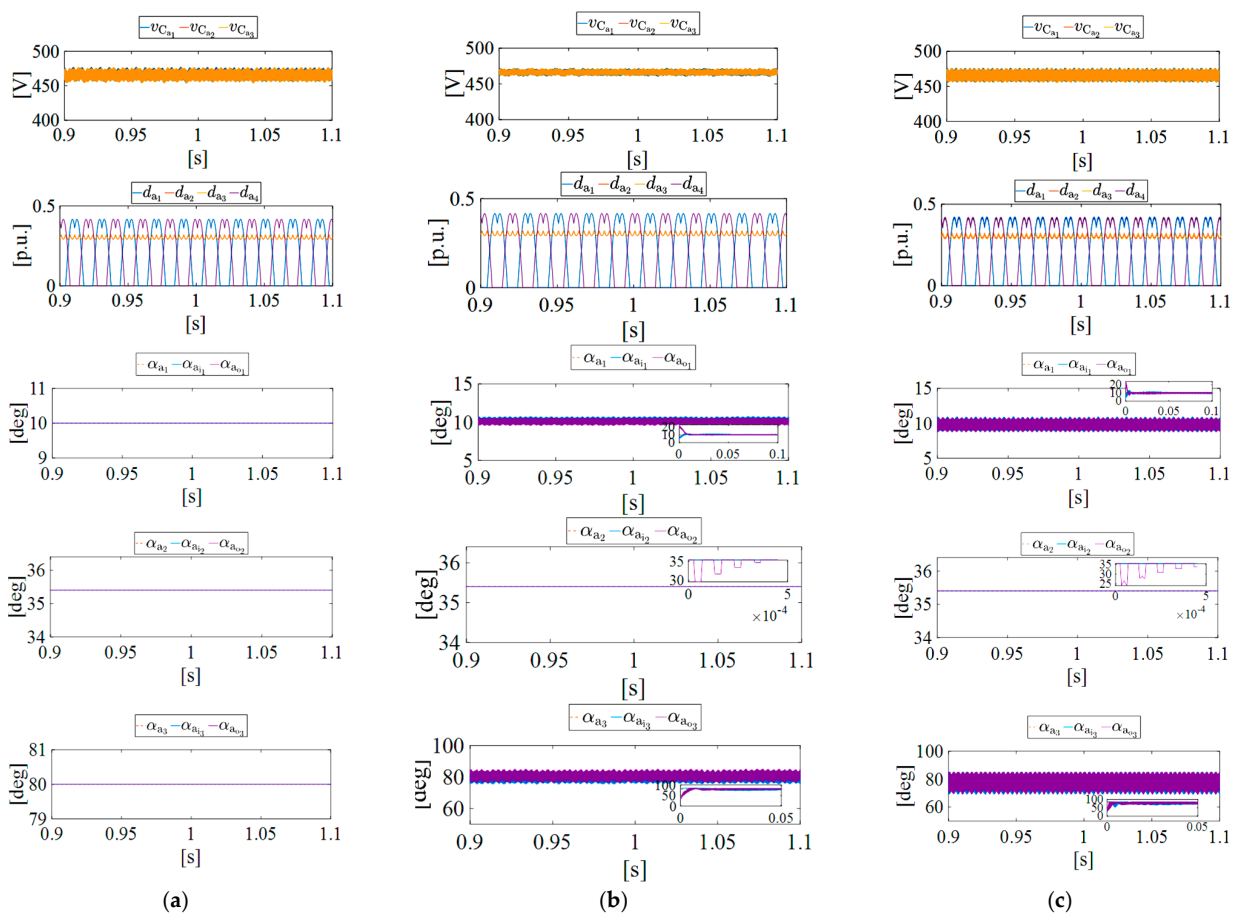


**Figure 15.** Bode plot and root locus diagram of the closed loop described in Figure 7e. (a) Bode plot of  $T_{\phi u}(s)$  (blue color) and  $T_{\phi}(s)$  (red color). (b) Root locus diagram of  $T_{\phi}(s)$ . Blue lines represent real-axis root evolution, while red and green curves track complex pole migration.

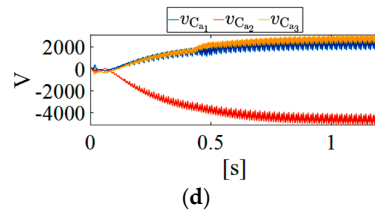
### 7.3. Time-Domain Simulation Results

In this subsection, the time-domain simulation results are presented for the proposed simulation scenarios and cases.

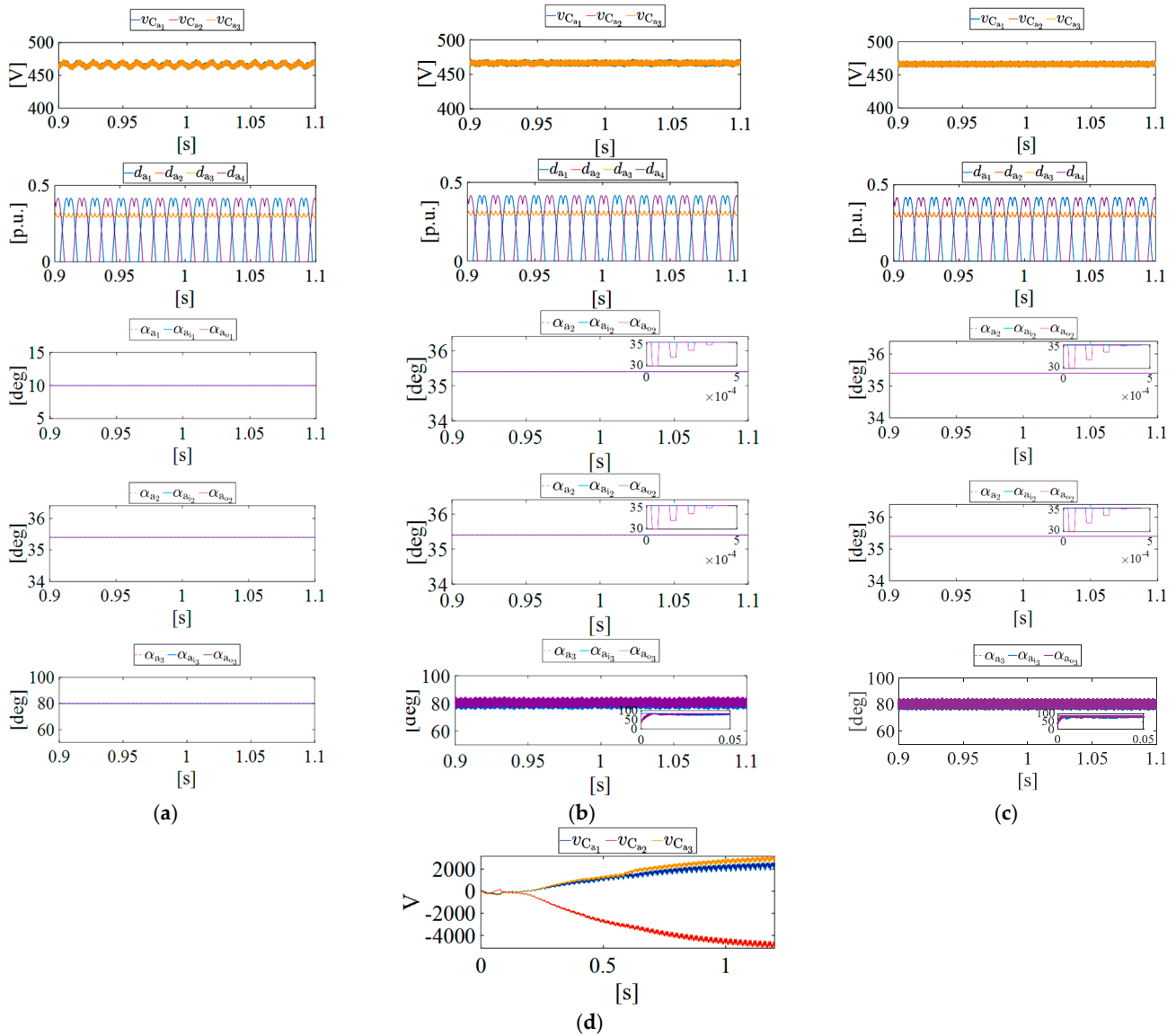
Figures 16–19 depict the value of voltages  $v_{Ca1}$ ,  $v_{Ca2}$ , and  $v_{Ca3}$ , leg “a” duty ratios  $d_{a1}$ ,  $d_{a2}$ ,  $d_{a3}$ , and  $d_{a4}$ , and switching angles corresponding to side a, i.e.,  $\alpha_{ajk}$  where  $j \in \{i, o\}$  and  $k \in \{1, 2, 3\}$ , with the system in steady-state operation, for scenarios 1 to 4, respectively. Figures 16a–c–19a–c correspond to cases 1 to 3, respectively. Additionally, Figures 16d–19d shows the dynamics of the voltages  $v_{Ca1}$ ,  $v_{Ca2}$ , and  $v_{Ca3}$  in the absence of balance control of these voltages.



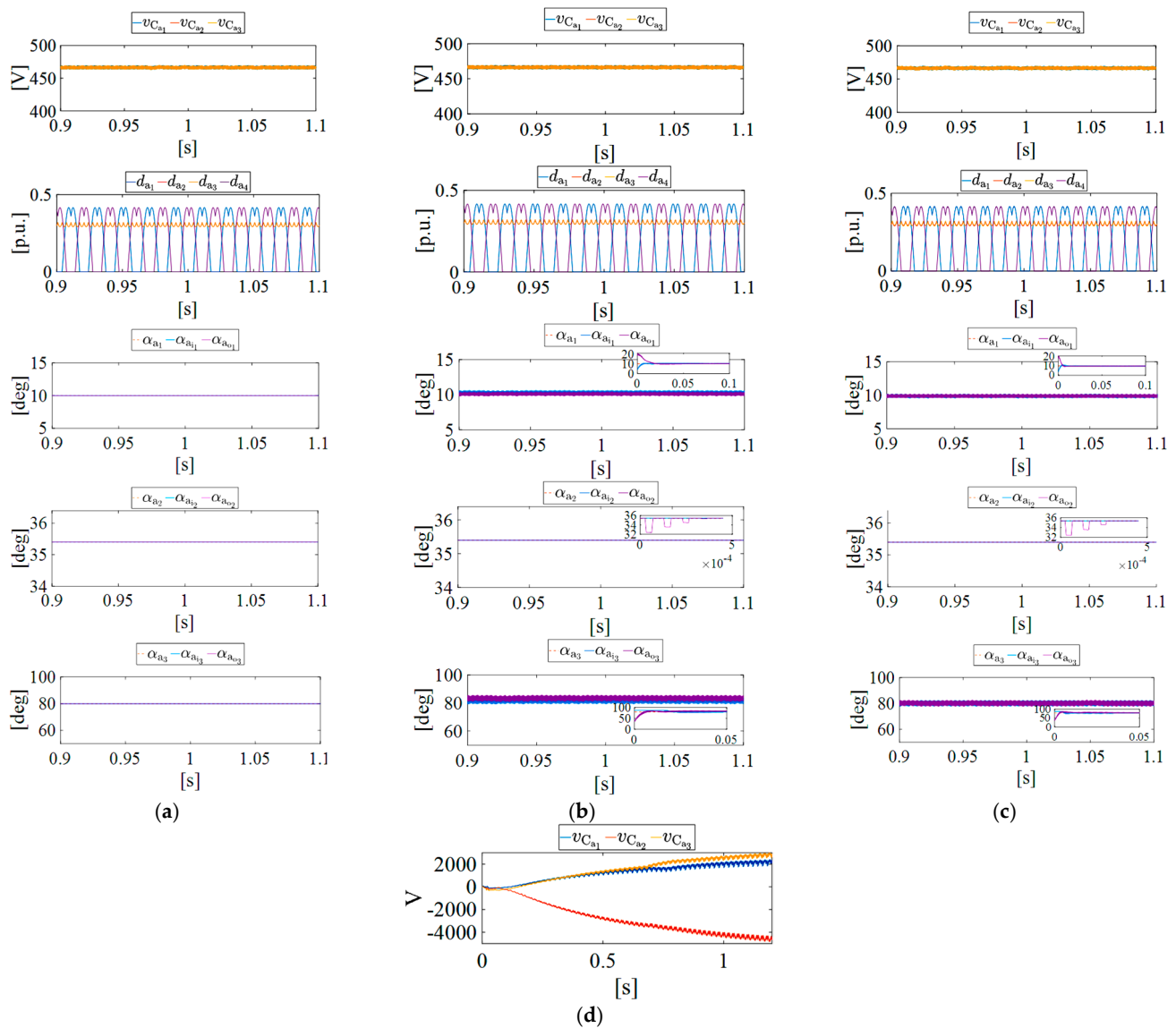
**Figure 16.** Cont.



**Figure 16.** Simulation of the 4L-BC under scenario 1 in steady-state operation. Initial voltages at start-up:  $v_{Ca10} = 280$  V,  $v_{Ca20} = 420$  V, and  $v_{Ca30} = 700$  V. Reference charging current:  $i_{B1}^* = i_{B2}^* = i_{B3}^* = 100$  A. Initial switching angles:  $\alpha_{z1} = 10^\circ$ ,  $\alpha_{z2} = 35.4^\circ$ , and  $\alpha_{z3} = 80^\circ$ , where  $z \in \{a, b\}$ . (a) Case 1. (b) Case 2. (c) Case 3. (d) Dynamics of  $v_{Ca1}$ ,  $v_{Ca2}$ , and  $v_{Ca3}$  in the absence of voltage balance control achieved by 4L-3P-NPC and 4L-1P-DAB.



**Figure 17.** Simulation of the 4L-BC under scenario 2 in steady-state operation. Initial voltages at start-up:  $v_{Ca10} = 280$  V,  $v_{Ca20} = 420$  V, and  $v_{Ca30} = 700$  V. Reference charging current:  $i_{B1}^* = i_{B2}^* = i_{B3}^* = 100$  A. Initial switching angles:  $\alpha_{z1} = 10^\circ$ ,  $\alpha_{z2} = 35.4^\circ$ , and  $\alpha_{z3} = 80^\circ$ , where  $z \in \{a, b\}$ . (a) Case 1. (b) Case 2. (c) Case 3. (d) Dynamics of  $v_{Ca1}$ ,  $v_{Ca2}$ , and  $v_{Ca3}$  in the absence of voltage balance control achieved by 4L-3P-NPC and 4L-1P-DAB.

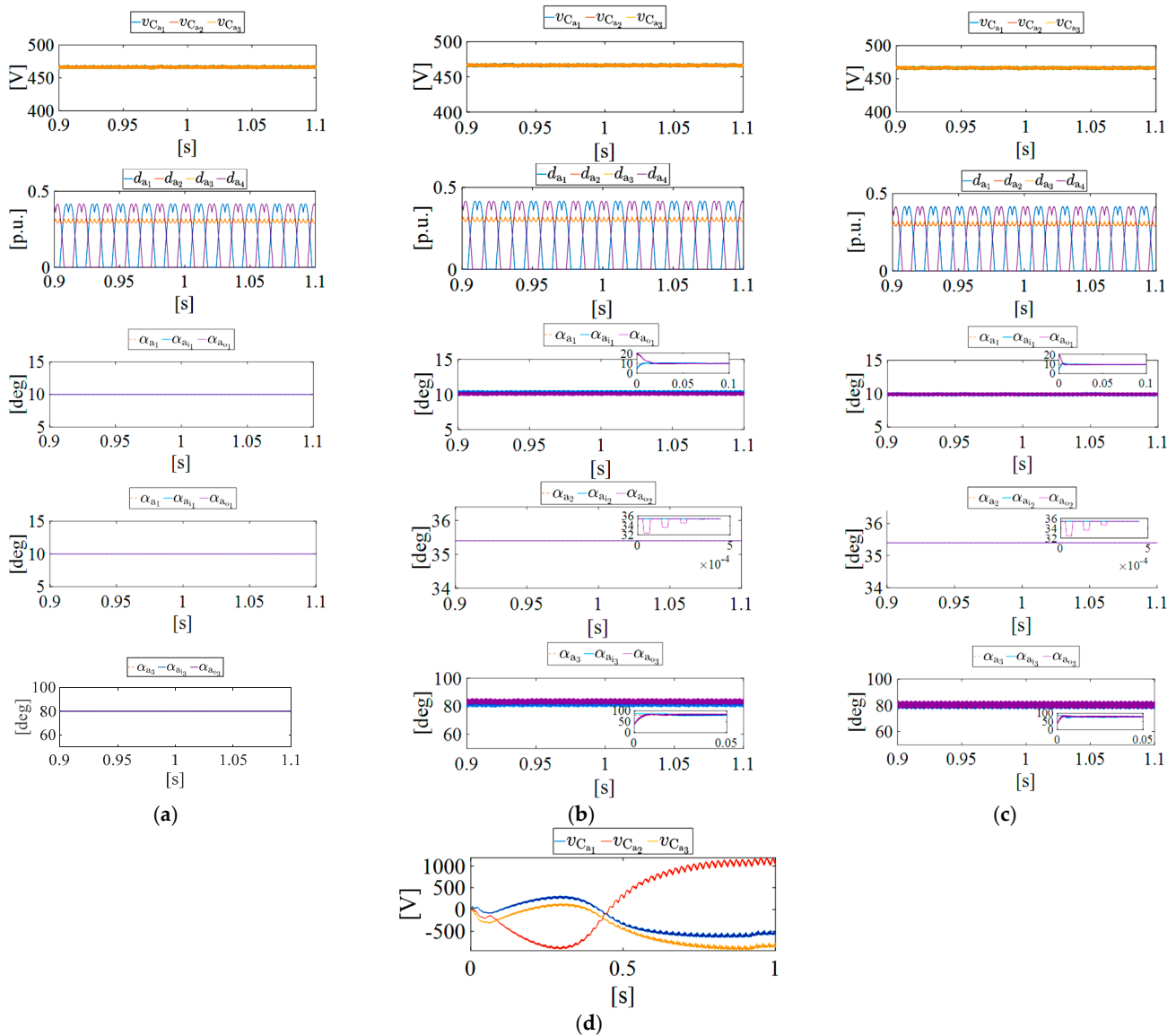


**Figure 18.** Simulation of the 4L-BC under scenario 3 in steady-state operation. Initial voltages at start-up:  $v_{Ca10} = 280$  V,  $v_{Ca20} = 420$  V, and  $v_{Ca30} = 700$  V. Reference charging current:  $i_{B1}^* = i_{B2}^* = i_{B3}^* = 100$  A. Initial switching angles:  $\alpha_{z1} = 10^\circ$ ,  $\alpha_{z2} = 35.4^\circ$ , and  $\alpha_{z3} = 80^\circ$ , where  $z \{a, b\}$ . (a) Case 1. (b) Case 2. (c) Case 3. (d) Dynamics of  $v_{Ca1}$ ,  $v_{Ca2}$ , and  $v_{Ca3}$  in the absence of voltage balance control achieved by 4L-3P-NPC and 4L-1P-DAB.

It is worth highlighting that the a-side DC-link voltage balance is essential for proper system operation. The first row in Figures 16–19 shows balanced a-side DC-link voltages in all conditions. To demonstrate the effectiveness of the balance control loop, the simulations in Figures 16d–19d were carried out with this control deactivated. Without balance control, the a-side DC-link voltages become unbalanced and reach unsafe values, which necessarily leads to a system shutdown to avoid system damage. It should be noted that the negative DC-link voltages shown in the simulation results would not be possible in a real system, since they will be clamped at zero by the converter diodes. Overall, it is obvious that the voltage balancing control loop is essential.

Under proper balanced operation, the high-frequency ripple observed in  $v_{Ca1}$ ,  $v_{Ca2}$ , and  $v_{Ca3}$  (first row in Figures 16–19) decreases with increasing capacitance from scenario 1 to 4, reflecting the filtering characteristics of the DC-link. In high-performance charging

systems, a ripple threshold of 1.5% is typically enforced, guiding the DC-link capacitor design for both energy storage and dynamic filtering.



**Figure 19.** Simulation of the 4L-BC under scenario 4 in steady-state operation. Initial voltages at start-up:  $v_{Ca10} = 280$  V,  $v_{Ca20} = 420$  V, and  $v_{Ca30} = 700$  V. Reference charging current:  $i_{B1}^* = i_{B2}^* = i_{B3}^* = 100$  A. Initial switching angles:  $\alpha_{z1} = 10^\circ$ ,  $\alpha_{z2} = 35.4^\circ$ , and  $\alpha_{z3} = 80^\circ$ , where  $z \in \{a, b\}$ . (a) Case 1. (b) Case 2. (c) Case 3. (d) Dynamics of  $v_{Ca1}$ ,  $v_{Ca2}$ , and  $v_{Ca3}$  in the absence of voltage balance control achieved by 4L-3P-NPC and 4L-1P-DAB.

A figure of merit (FoM) related to the values of the percentage of ripple in the DC-link voltages ( $rr_{vca1}$ ,  $rr_{vca2}$ , and  $rr_{vca3}$ ) are calculated and summarized in Table 4. Figures 16–19 confirm that this requirement is not satisfied in scenario 1 except for  $v_{Ca2}$  in case 2, as detailed in Table 4. The ripple performance improves substantially in scenarios 3 and 4, meeting specifications across all cases. The peak ripple is observed in  $rr_{vca1}$  for scenario 1, case 3, whereas the lowest ripple appears in  $rr_{vca2}$  for scenario 4.

**Table 4.** Percentage of ripple in the a-side DC-link voltages ( $rr_{vCa1}$ ,  $rr_{vCa2}$ , and  $rr_{vCa3}$ ).

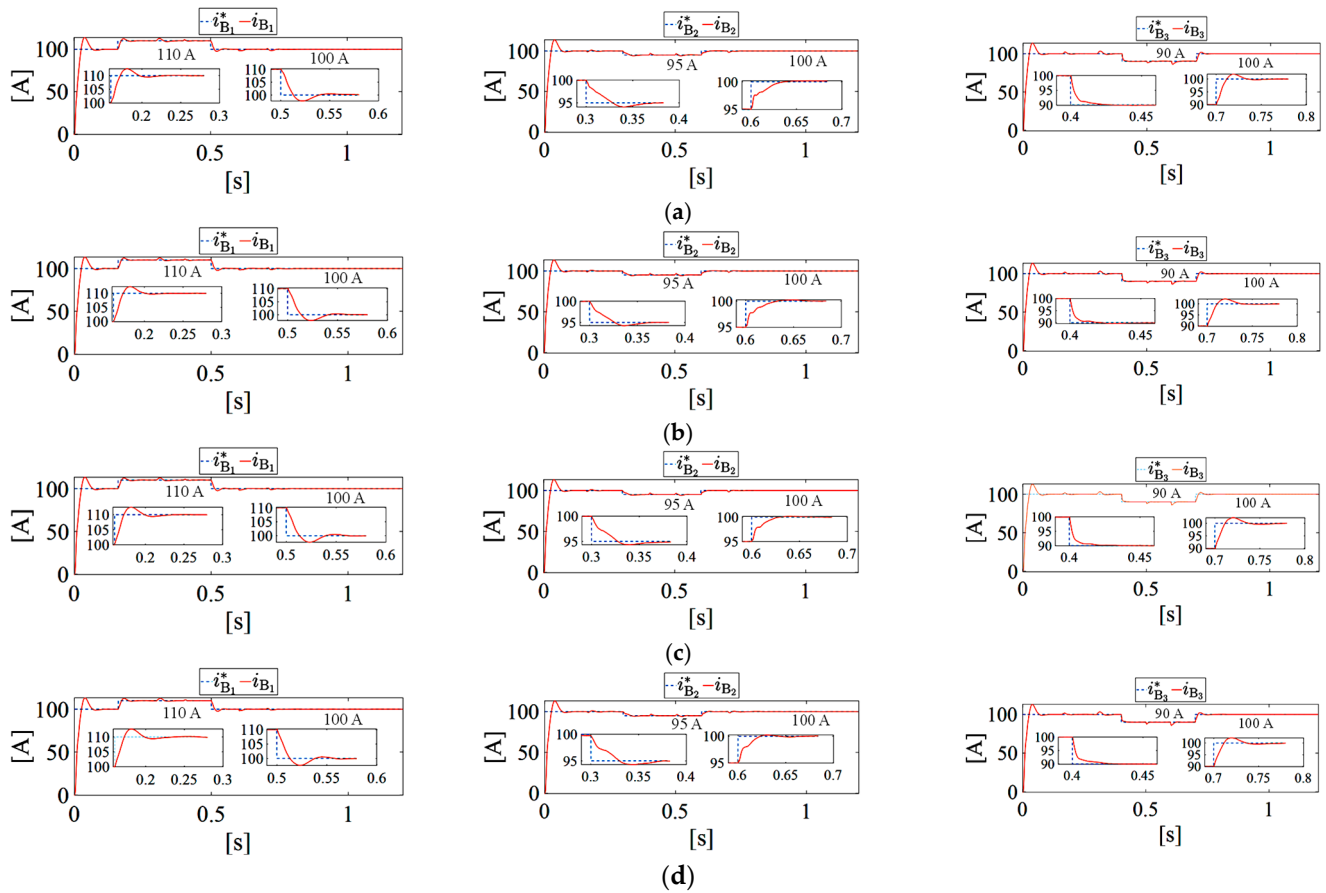
Scenarios	$rr_{vCa1}$ , $rr_{vCa2}$ , and $rr_{vCa3}$ in [%]	Cases		
		1	2	3
1	$rr_{vCa1}$	3.77	1.90	3.89
	$rr_{vCa2}$	0.75	0.65	0.83
	$rr_{vCa3}$	3.36	1.97	3.30
2	$rr_{vCa1}$	1.87	1.65	1.65
	$rr_{vCa2}$	0.47	0.24	0.30
	$rr_{vCa3}$	1.70	1.58	1.67
3	$rr_{vCa1}$	1.43	1.37	1.28
	$rr_{vCa2}$	0.26	0.23	0.26
	$rr_{vCa3}$	1.28	1.45	1.48
4	$rr_{vCa1}$	1.00	0.86	1.03
	$rr_{vCa2}$	0.21	0.21	0.21
	$rr_{vCa3}$	0.88	0.90	0.90

The duty ratios of the AC-DC converter legs do not reach saturation under any scenario or case, preserving control margin and suggesting that DC-link capacitance could potentially be reduced without compromising dynamic controllability.

From Figures 16a–19a (case 1 in all scenarios), it is observed that the switching angles are kept constant around their reference values, i.e.,  $\alpha_{a1} = 10^\circ$ ,  $\alpha_{a2} = 35.4^\circ$ , and  $\alpha_{a3} = 80^\circ$ , which is consistent, since in this case, the 4L-1P-DAB controllers are not responsible for regulating the balance of the a-side DC-link voltages, and therefore, these controllers are not generating any control effort. Additionally, it should be noted that the angles values were calculated in accordance with [25] to guarantee that the currents flowing through the internal points of the a-side DC-link as seen from the 4L-1P-DAB converter, i.e.,  $i_{2a}$  and  $i_{3a}$ , provide a null electrical charge. However, in cases 2 and 3 of all scenarios (see Figures 16b,c–19b,c), one can see the control efforts produced by the controllers, which is convincing since, in these cases, the 4L-1P-DAB converter is in charge of regulating the balance of the a-side DC-link voltages. It is evident from Figures 16b–19b that the angles  $\alpha_{amn}$ , where  $m \in \{i, o\}$  and  $n \in \{1, 2, 3\}$ , approach their  $\alpha_{an}$  reference values. Thus, the 4L-1P-DAB converter can operate with the balanced voltages of the a-side DC-link capacitors. Moreover, it can be seen that the  $\alpha_{amn}$  dynamics present variations with respect to their reference values, with the largest one seen in  $\alpha_{am1}$  and  $\alpha_{am3}$ . Also, the angle  $\alpha_{a3}$  saturates at  $90^\circ$ . The 4L-1P-DAB converter has the same control margin and can eventually enable a reduction in the capacity of the a-side DC-link. Finally, the control efforts generated by the 4L-1P-DAB converter when the system operates in cases 2 and 3 are greater as the capacity of the a-side DC-link decreases.

It should be noted that during the execution of the 4L-BC case studies, the tuning parameters of the compensators related to the balancing of the a-side DC-link voltages, as well as those related to the regulation of the CM and DM components, were not modified, which means that the developed tuning process was performed satisfactorily.

Figure 20 shows the dynamics under step changes in the charging currents ( $i_{Bx}$ ,  $x \in \{1, 2, 3\}$ ) in case 3, for all scenarios. Figure 20a–d relate to scenarios 1–4, respectively.



**Figure 20.** Simulation of battery current control transients under case 3. Initial voltages:  $v_{Ca10} = 280$  V,  $v_{Ca20} = 420$  V, and  $v_{Ca30} = 700$  V. Reference charging current:  $i_{B1}^* = i_{B2}^* = i_{B3}^* = 100$  A. Step change in  $i_{B1}^*$  at 160 ms and 500 ms. Step change in  $i_{B2}^*$  at 300 ms and 600 ms. Step change in  $i_{B3}^*$  at 400 ms and 700 ms. (a) Scenario 1. (b) Scenario 2. (c) Scenario 3. (d) Scenario 4.

At start-up, the reference currents ( $i_{B1}^*$ ,  $i_{B2}^*$ , and  $i_{B3}^*$ ) are set to 100 A. At 160 ms,  $i_{B1}^*$  takes the value of 110 A and the other currents remain at their initial reference values. Subsequently, at 300 ms,  $i_{B2}^*$  takes the value of 95 A whereas  $i_{B1}$  and  $i_{B3}$  are maintained at 110 A and 100 A, respectively. Then, at 400 ms,  $i_{B3}^*$  is set to 90 A and  $i_{B1}$  and  $i_{B2}$  are maintained at 110 A and 95 A, respectively. Finally, at 500 ms, 600 ms, and 700 ms, the currents  $i_{B1}^*$ ,  $i_{B2}^*$ , and  $i_{B3}^*$  return to their initial reference values, i.e., 100 A, respectively. From Figure 20, it can be seen that the maximum start-up overshoot for each scenario is approximately equal to 7.5%, which represents a relatively low value. In addition, two other FoMs are defined, i.e., the overshoot and settling time. On the other hand, a second constraint was imposed on the system and it is related to the maximum percentage overshoot allowed, which is set to 10%, a typical value in the literature [34,35,37].

The FoMs related to  $i_{Bx}$  are summarized in Table 5 according to Figure 20. Table 5, derived from Figure 20, succinctly presents the FoMs pertaining to  $i_{Bx}$  (where  $x \in \{1, 2, 3\}$ ).

A comprehensive analysis of the results in Table 5 reveals patterns in the maximum and minimum values of overshoots and settling times. With respect to the step change time and  $i_{Bx}$  reference, the maximum values are as follows: 3.46% (scenario 1), 0.79% (scenario 4), 1.28% (scenario 1), 0.77% (scenario 4), 1.75% (scenario 1), and 1.92% (scenario 4), and 97.82 ms (scenario 3), 85.32 ms (scenario 3), 81.68 ms (scenario 4), 55.66 ms (scenario 3), 60.83 ms (scenario 2), and 72.27 ms (scenario 4) for step change times of 160 ms, 300 ms, 400 ms, 400 ms, 500 ms, 600 ms, and 700 ms, respectively.

**Table 5.** Summary of overshoots and settling times in step changes in charging currents.

Step Change Time [ms]	Step Change Current	FoM	Scenarios		
			1	2	3
160	$i_{B1}^*$	Overshoot [%]	3.46	3.33	3.02
		Settling time [ms]	91.50	97.74	97.82
300	$i_{B2}^*$	Overshoot [%]	0.77	0.76	0.78
		Settling time [ms]	85.12	85.25	85.32
400	$i_{B3}^*$	Overshoot [%]	1.28	1.11	0.95
		Settling time [ms]	81.35	81.32	81.57
500	$i_{B1}^*$	Overshoot [%]	0.69	0.72	0.76
		Settling time [ms]	52.71	52.63	55.66
600	$i_{B2}^*$	Overshoot [%]	1.75	1.65	1.23
		Settling time [ms]	60.75	60.83	60.81
700	$i_{B3}^*$	Overshoot [%]	1.69	1.61	1.17

Conversely, the minimum values for overshoots and settling times, also in relation to the step change time and  $i_{Bx}$  reference, are 2.84% (scenario 4), 0.76% (scenario 2), 0.94% (scenario 4), 0.69% (scenario 1), 1.01% (scenario 4), and 1.17% (scenario 3), and 91.50 ms (scenario 1), 85.12 ms (scenario 1), 81.32 ms (scenario 2), 52.63 ms (scenario 2), 60.58 ms (scenario 4), and 72.13 ms (scenario 1) for step change times of 160 ms, 300 ms, 400 ms, 400 ms, 500 ms, 600 ms, and 700 ms, respectively.

Upon careful examination of the maximum and minimum results, organized by step change time and  $i_{Bx}$ , it is evident that the highest values for overshoots and settling times across all scenarios are 3.46% (scenario 1, step change @ 160 ms) and 97.82 ms (scenario 3, step change @ 160 ms), respectively. Conversely, the lowest values are 0.69% (scenario 1, step change @ 500 ms) and 52.63 ms (scenario 2, step change @ 500 ms). In summary, the 4L-BC demonstrates effective controllability of  $i_{Bx}$  in all scenarios, characterized by favorable FoMs and negligible steady-state errors.

## 8. Conclusions

This work constitutes proof-of-concept of a novel four-level battery charger based on an extended dual-active-bridge converter topology, which has not been previously studied in the literature. This multibattery charging system is based on a hybrid multilevel topology by combining a four-level three-phase neutral-point-clamped (4L-3P-NPC) AC-DC converter and a four-level single-phase dual-active-bridge (4L-1P-DAB) DC-DC converter.

A comprehensive analytical model was developed, including the switching-level representation, large-signal averaged models in time and D-Q domains, and a small-signal linear state-space model. These models accurately describe the system dynamics—including DC-link voltage regulation, multibattery current control, power transfer, and capacitor voltage balancing—and enable classical control design and frequency-domain stability analysis using gain/phase margin criteria.

The proposed multiloop control system fulfills three primary objectives: (i) the regulation of the total a-side DC-link voltage and reactive power control via the 4L-3P-NPC stage, (ii) the precise control of individual battery pack charging/discharging currents via the 4L-1P-DAB stage, and (iii) active voltage balancing across the a-side and b-side DC-link capacitors. Modulation strategies include virtual-vector PWM (VVPWM) for the NPC stage and a multilevel angle-based strategy for the DAB stage, both contributing to enhanced harmonic performance and DC-link capacitor voltage balancing.

The proposed system was successfully validated by simulation with MATLAB/Simulink. The stability analysis of the compensated control loops confirms gain and phase margins well above design thresholds across all control domains. Time-domain simulations validate the proposed system under a wide range of capacitance scenarios and dynamic loading conditions. The results confirm fast transient response (settling times < 100 ms), low overshoot (<3.5%), high disturbance rejection, negligible steady-state error, and efficient ripple suppression, with ripple percentages below 1.5% in most cases. Furthermore, tuning parameters remained fixed across all tested conditions, evidencing the robustness and generalizability of the control strategy.

A key advantage of the proposed architecture lies in its modularity and scalability. The system is naturally extendable to more battery packs or higher DC-link voltage levels configurations without requiring significant structural changes.

The advantages of multilevel converters in comparison to conventional two-level converters are well known and will not be detailed here. However, they require DC-link capacitor voltage balance to guarantee correct operation. In the proposed system, DC-link capacitor voltage balance is achieved by means of a dual control strategy, in which both the 4L-3P-NPC and 4L-1P-DAB converters are responsible for balancing the a-side DC-link.

From the point of view of the battery, the four-level converter enables the use of a battery bank consisting of three battery packs connected in series. The simulation results show that the proposed control approach allows the current of each battery pack to be controlled. This feature is very interesting, as it allows the state-of-charge of the battery packs to be balanced and enables the use of battery packs with different charge levels. Moreover, it is feasible to work with battery packs that have different loading or varying degrees of aging, are built with different chemistries, and even combine new and second-life battery packs, thus maximizing the available capacity of the battery bank.

Future work will focus on the experimental validation of the proposed 4L-BC system, including hardware-in-the-loop testing and full-scale prototype development. Further experimental analyses, for instance, the analysis of the power losses, system overall efficiency, power loss distribution, or power quality, among others, will be useful to quantify the benefits of the proposed battery charger compared to current chargers.

Finally, it should be noted that the proposed battery charger combines the advantages provided by multilevel converters, the flexible and compact behavior of the dual-active-bridge converter, and customized battery pack charging. These advantages make the proposed system a suitable, feasible, and promising option for implementing battery chargers, in applications such as heavy-duty electric vehicles, second-life battery repurposing, stationary storage, and vehicle-to-everything (V2X) scenarios.

**Author Contributions:** Conceptualization, J.M.C.-S., S.B.-M. and A.F.-M.; methodology, J.M.C.-S., S.B.-M. and A.F.-M.; validation, J.M.C.-S., S.B.-M., A.F.-M. and S.A.; formal analysis, J.M.C.-S., S.B.-M., A.F.-M. and S.A.; investigation, J.M.C.-S., S.B.-M., A.F.-M. and S.A.; writing—original draft preparation, J.M.C.-S.; writing—review and editing, S.B.-M., A.F.-M. and S.A.; supervision, S.A.; funding acquisition, S.B.-M. All authors have read and agreed to the published version of the manuscript.

**Funding:** This publication is part of Grant PID2022-138384NB-I00, funded by MCIN/AEI/10.13039/501100011033 and by ERDF A way of making Europe.

**Data Availability Statement:** The original contributions presented in this study are included in the article, and further inquiries can be directed to the corresponding author.

**Conflicts of Interest:** The authors declare no conflicts of interest.

## Appendix A

In the following, the corresponding set of equations and transfer functions are included. The description for all these equations is given here at the beginning of this appendix. More detailed information is found in [38].

The state matrix in (1) is defined as (A1) and the matrix  $\mathbf{B}_1$  can be defined as (A2).

The matrices associated with the 4L-1P-DAB converter model shown in (4) are defined in (A3) and (A4).

Regarding the battery bank model, the matrix  $\mathbf{B}_3$  in (8) is defined as (A5).

The submatrices  $\mathbf{A}_{jk}$ ,  $\mathbf{B}_{jk}$ ,  $\mathbf{B}_{12}$ , and  $\mathbf{B}_{22}$ , which are associated with the linear model of the submatrices in (19), are defined in (A6) and (A7). The constants  $K$  appearing in the transfer functions in (21) are defined in (A8).

The explicit mathematical expressions of the transfer functions (TFs) referenced throughout Section 6.5 are shown as follows. These TFs are derived from the small-signal linear model of the 4L-BC system described in Section 5 and represent the core dynamics of each control loop within the system.

The plant transfer function of the outer voltage regulation loop is defined in (A9). The d- and q-axis current control loops share the same second-order transfer function defined in (A10). The two balancing loops designed to regulate the imbalance among the three capacitors of the a-side DC-link are defined in (A11). Also, the transfer functions for the differential-mode current regulation loops are modeled as (A12). Finally, the common-mode current control loop regulates the total power transfer via the modulation angle  $\phi$  which is presented in (A13). Here,  $K_\phi$  is the gain dependent on modulation indices and the transformer turn ratio.  $\omega_{pi}$  and  $\omega_z$  are the dominant poles and the right-half-plane zero due to the non-minimum phase characteristic.

$$\mathbf{A}_1(t) = \begin{matrix} \\ = \end{matrix} \begin{bmatrix} -\frac{R_{ac}}{L_{ac}} & 0 & 0 & \frac{-2 \cdot s_{a1a} + s_{b1a} + s_{c1a}}{3 \cdot L_{ac}} & \frac{2 \cdot (s_{a3a} + s_{a4a}) - (s_{b3a} + s_{b4a}) - (s_{c3a} + s_{c4a})}{3 \cdot L_{ac}} & \frac{2 \cdot s_{a4a} - s_{b4a} - s_{c4a}}{3 \cdot L_{ac}} \\ 0 & -\frac{R_{ac}}{L_{ac}} & 0 & \frac{s_{a1a} - 2 \cdot s_{b1a} + s_{c1a}}{3 \cdot L_{ac}} & \frac{-(s_{a3a} + s_{a4a}) + 2 \cdot (s_{b3a} + s_{b4a}) - (s_{c3a} + s_{c4a})}{3 \cdot L_{ac}} & \frac{-s_{a4a} + 2 \cdot s_{b4a} - s_{c4a}}{3 \cdot L_{ac}} \\ 0 & 0 & -\frac{R_{ac}}{L_{ac}} & \frac{s_{a1a} + s_{b1a} - 2 \cdot s_{c1a}}{3 \cdot L_{ac}} & \frac{-s_{a3a} - s_{b3a} + 2 \cdot s_{c3a}}{3 \cdot L_{ac}} & \frac{-s_{a4a} - s_{b4a} + 2 \cdot s_{c4a}}{3 \cdot L_{ac}} \\ -\frac{1 - s_{a1a}}{C_a} & -\frac{1 - s_{b1a}}{C_a} & -\frac{1 - s_{c1a}}{C_a} & -\frac{1}{R_{C_a} \cdot C_a} & 0 & 0 \\ -\frac{s_{a3a}}{C_a} & -\frac{s_{b3a}}{C_a} & -\frac{s_{c3a}}{C_a} & 0 & -\frac{1}{R_{C_a} \cdot C_a} & 0 \\ -\frac{s_{a4a}}{C_a} & -\frac{s_{b4a}}{C_a} & -\frac{s_{c4a}}{C_a} & 0 & 0 & -\frac{1}{R_{C_a} \cdot C_a} \end{bmatrix} \quad (A1)$$

$$\mathbf{B}_1 = \begin{bmatrix} -\frac{2}{3 \cdot L_{ac}} & \frac{1}{3 \cdot L_{ac}} & \frac{1}{3 \cdot L_{ac}} & 0 & 0 & 0 \\ \frac{1}{3 \cdot L_{ac}} & -\frac{2}{3 \cdot L_{ac}} & \frac{1}{3 \cdot L_{ac}} & 0 & 0 & 0 \\ \frac{1}{3 \cdot L_{ac}} & \frac{1}{3 \cdot L_{ac}} & -\frac{2}{3 \cdot L_{ac}} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -\frac{1}{C_a} & -\frac{1}{C_a} \\ 0 & 0 & 0 & 0 & 0 & -\frac{1}{C_a} \end{bmatrix} \quad (A2)$$

$$\begin{aligned}
 & \mathbf{A}_2(t) = \\
 = & \begin{bmatrix} -\frac{1}{R_{C_a} \cdot C_a} & 0 & 0 & -\frac{s_{a2T} + s_{a3T} + s_{a4T}}{C_a} & 0 & 0 & 0 & 0 & 0 \\ 0 & -\frac{1}{R_{C_a} \cdot C_a} & 0 & -\frac{s_{a3T} + s_{a4T}}{C_a} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{R_{C_a} \cdot C_a} & -\frac{s_{a4T}}{C_a} & 0 & 0 & 0 & 0 & 0 \\ -\frac{s_{a1T}}{L_k} & \frac{s_{a3T} + s_{a4T}}{L_k} & \frac{s_{a4T}}{L_k} & -\frac{R_{L_k}}{L_k} & 0 & 0 & 0 & -\frac{a_{tr} \cdot (s_{b3T} + s_{b4T})}{L_k} & -\frac{a_{tr} \cdot s_{b4T}}{L_k} \\ 0 & 0 & 0 & 0 & 0 & 0 & -\frac{a_{tr} \cdot s_{b1T}}{L_m} & \frac{a_{tr} \cdot (s_{b3T} + s_{b4T})}{L_m} & \frac{a_{tr} \cdot s_{b4T}}{L_m} \\ \frac{a_{tr} \cdot s_{a1T}}{L_k} & -\frac{a_{tr} \cdot (s_{a3T} + s_{a4T})}{L_k} & -\frac{a_{tr} \cdot s_{a4T}}{L_k} & \frac{a_{tr} \cdot R_{L_k}}{L_k} & 0 & 0 & -\frac{a_{tr}^2 \cdot s_{b1T}}{L_k || L_m} & \frac{a_{tr}^2 \cdot (s_{b3T} + s_{b4T})}{L_k || L_m} & \frac{a_{tr}^2 \cdot s_{b4T}}{L_k || L_m} \\ 0 & 0 & 0 & 0 & 0 & -\frac{s_{b2T} + s_{b3T} + s_{b4T}}{C_b} & -\frac{1}{R_{C_b} \cdot C_b} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & -\frac{s_{b3T} + s_{b4T}}{C_b} & 0 & -\frac{1}{R_{C_b} \cdot C_b} & 0 \\ 0 & 0 & 0 & 0 & 0 & -\frac{s_{b4T}}{C_b} & 0 & 0 & -\frac{1}{R_{C_b} \cdot C_b} \end{bmatrix} \tag{A3}
 \end{aligned}$$

$$\mathbf{B}_2 = \begin{bmatrix} -\frac{1}{C_a} & -\frac{1}{C_a} & -\frac{1}{C_a} & 0 & 0 & 0 \\ 0 & -\frac{1}{C_a} & -\frac{1}{C_a} & 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{C_a} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{C_b} & -\frac{1}{C_b} & -\frac{1}{C_b} \\ 0 & 0 & 0 & 0 & -\frac{1}{C_b} & -\frac{1}{C_b} \\ 0 & 0 & 0 & 0 & 0 & -\frac{1}{C_b} \end{bmatrix} \tag{A4}$$

$$\mathbf{B}_3 = \begin{bmatrix} 1 & 0 & 0 & -1 & 0 & 0 \\ 0 & 1 & 0 & 1 & -1 & 0 \\ 0 & 0 & 1 & 0 & 0 & -1 \end{bmatrix} \tag{A5}$$

$$\begin{aligned}
 & \mathbf{A}_{11} = \\
 = & \begin{bmatrix} -\frac{R_{ac}}{L_{ac}} & \omega & 0 & 0 \\ -\omega & -\frac{R_{ac}}{L_{ac}} & 0 & 0 \\ -\frac{V_d}{C_a \cdot V_{dca}} & -\frac{V_q}{C_a \cdot V_{dca}} & \frac{I_d \cdot V_d}{C_a \cdot V_{dca}^2} - \frac{1}{C_a} \cdot \left( \frac{1}{R_{C_a}} + \frac{K_a^2 \cdot R_{L_k}}{|Z_k(j \cdot \omega_s)|^2} \right) & \frac{V_d \cdot I_d}{C_a \cdot V_{dca}^2} - \frac{K_a^2 \cdot R_{L_k}}{C_a \cdot |Z_k(j \cdot \omega_s)|^2} \\ -\frac{V_d}{C_a \cdot V_{dca}} & -\frac{V_q}{C_a \cdot V_{dca}} & \frac{V_d \cdot I_d}{C_a \cdot V_{dca}^2} - \frac{K_a^2 \cdot R_{L_k}}{C_a \cdot |Z_k(j \cdot \omega_s)|^2} & \frac{I_d \cdot V_d}{C_a \cdot V_{dca}^2} - \frac{1}{C_a} \cdot \left( \frac{1}{R_{C_a}} + \frac{K_a^2 \cdot R_{L_k}}{|Z_k(j \cdot \omega_s)|^2} \right) \\ -\frac{V_d}{C_a \cdot V_{dca}} & -\frac{V_q}{C_a \cdot V_{dca}} & \frac{V_d \cdot I_d}{C_a \cdot V_{dca}^2} - \frac{K_a^2 \cdot R_{L_k}}{C_a \cdot |Z_k(j \cdot \omega_s)|^2} & \frac{V_d \cdot I_d}{C_a \cdot V_{dca}^2} - \frac{K_a^2 \cdot R_{L_k}}{C_a \cdot |Z_k(j \cdot \omega_s)|^2} \\ 0 & 0 & \frac{1}{C_b \cdot |Z_k(j \cdot \omega_s)|^2} \cdot \left( 2 \cdot \frac{K_a^2 \cdot R_{L_k} \cdot V_{dca}}{V_{dcb}} - a_{tr} \cdot K_a \cdot K_b \cdot |Z_k(j \cdot \omega_s)| \cdot \sin(\varphi - \sigma) \right) & \frac{1}{C_b \cdot |Z_k(j \cdot \omega_s)|^2} \cdot \left( 2 \cdot \frac{K_a^2 \cdot R_{L_k} \cdot V_{dca}}{V_{dcb}} - a_{tr} \cdot K_a \cdot K_b \cdot |Z_k(j \cdot \omega_s)| \cdot \sin(\varphi - \sigma) \right) \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \frac{V_d \cdot I_d}{C_a \cdot V_{dca}^2} - \frac{K_a^2 \cdot R_{L_k}}{C_a \cdot |Z_k(j \cdot \omega_s)|^2} & \frac{V_d \cdot I_d}{C_a \cdot V_{dca}^2} - \frac{K_a^2 \cdot R_{L_k}}{C_a \cdot |Z_k(j \cdot \omega_s)|^2} & \frac{a_{tr} \cdot K_a \cdot K_b \cdot \sin(\varphi - \sigma)}{C_a \cdot |Z_k(j \cdot \omega_s)|} & \frac{a_{tr} \cdot K_a \cdot K_b \cdot \sin(\varphi - \sigma)}{C_a \cdot |Z_k(j \cdot \omega_s)|} \\ \frac{V_d \cdot I_d}{C_a \cdot V_{dca}^2} - \frac{K_a^2 \cdot R_{L_k}}{C_a \cdot |Z_k(j \cdot \omega_s)|^2} & \frac{V_d \cdot I_d}{C_a \cdot V_{dca}^2} - \frac{K_a^2 \cdot R_{L_k}}{C_a \cdot |Z_k(j \cdot \omega_s)|^2} & \frac{a_{tr} \cdot K_a \cdot K_b \cdot \sin(\varphi - \sigma)}{C_a \cdot |Z_k(j \cdot \omega_s)|} & \frac{a_{tr} \cdot K_a \cdot K_b \cdot \sin(\varphi - \sigma)}{C_a \cdot |Z_k(j \cdot \omega_s)|} \\ \frac{I_d \cdot V_d}{C_a \cdot V_{dca}^2} - \frac{1}{C_a} \cdot \left( \frac{1}{R_{C_a}} + \frac{K_a^2 \cdot R_{L_k}}{|Z_k(j \cdot \omega_s)|^2} \right) & \frac{I_d \cdot V_d}{C_a \cdot V_{dca}^2} - \frac{1}{C_a} \cdot \left( \frac{1}{R_{C_a}} + \frac{K_a^2 \cdot R_{L_k}}{|Z_k(j \cdot \omega_s)|^2} \right) & \frac{a_{tr} \cdot K_a \cdot K_b \cdot \sin(\varphi - \sigma)}{C_a \cdot |Z_k(j \cdot \omega_s)|} & \frac{a_{tr} \cdot K_a \cdot K_b \cdot \sin(\varphi - \sigma)}{C_a \cdot |Z_k(j \cdot \omega_s)|} \\ \frac{1}{C_b \cdot |Z_k(j \cdot \omega_s)|^2} \cdot \left( 2 \cdot \frac{K_a^2 \cdot R_{L_k} \cdot V_{dca}}{V_{dcb}} - a_{tr} \cdot K_a \cdot K_b \cdot |Z_k(j \cdot \omega_s)| \cdot \sin(\varphi - \sigma) \right) & \frac{1}{C_b \cdot |Z_k(j \cdot \omega_s)|^2} \cdot \left( 2 \cdot \frac{K_a^2 \cdot R_{L_k} \cdot V_{dca}}{V_{dcb}} - a_{tr} \cdot K_a \cdot K_b \cdot |Z_k(j \cdot \omega_s)| \cdot \sin(\varphi - \sigma) \right) & -\frac{1}{C_b} \cdot \left( \frac{1}{R_{C_b}} + \frac{R_{L_k}}{V_{dcb}^2} + \frac{K_a^2 \cdot R_{L_k} \cdot V_{dca}^2}{V_{dcb}^2 \cdot |Z_k(j \cdot \omega_s)|^2} \right) & -\frac{1}{C_b} \cdot \left( \frac{1}{R_{C_b}} + \frac{R_{L_k}}{V_{dcb}^2} + \frac{K_a^2 \cdot R_{L_k} \cdot V_{dca}^2}{V_{dcb}^2 \cdot |Z_k(j \cdot \omega_s)|^2} \right) \end{bmatrix}
 \end{aligned}$$



$$\mathbf{B}_{21} = \mathbf{0}$$

$$\mathbf{B}_{22} = \begin{bmatrix} 0 & -\frac{V_{C_{b1}}}{C_b \cdot V_{d_{c_b}}} & \frac{V_{C_{b3}}}{C_b \cdot V_{d_{c_b}}} & 0 & 0 & 0 & \frac{a_{tr} \cdot K_a \cdot K_b \cdot V_{d_{c_a}} \cdot \sin(\varphi + v)}{C_b \cdot |Z_k(j \cdot \omega_s)|} \\ 0 & -\frac{V_{C_{b1}}}{C_b \cdot V_{d_{c_b}}} & -\frac{(V_{C_{b1}} + V_{C_{b2}})}{C_b \cdot V_{d_{c_b}}} & 0 & 0 & 0 & \frac{a_{tr} \cdot K_a \cdot K_b \cdot V_{d_{c_a}} \cdot \sin(\varphi + v)}{C_b \cdot |Z_k(j \cdot \omega_s)|} \\ 0 & 0 & 0 & -\frac{1}{L_{dc}} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -\frac{1}{L_{dc}} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & -\frac{1}{L_{dc}} & 0 \end{bmatrix} \tag{A7}$$

$$K_1 = \frac{R_{ac}}{L_{ac}}, K_2 = \omega, K_3 = \frac{1}{L_{ac}}, K_4 = \frac{V_d}{C_a \cdot V_{d_{c_a}}}, K_5 = \frac{V_q}{C_a \cdot V_{d_{c_a}}},$$

$$K_6 = \frac{V_{d_{c_a}}^2 - R_{c_a} \cdot V_d \cdot V_q}{C_a \cdot R_{c_a} \cdot V_{d_{c_a}}^2} + \frac{K_a^2 \cdot R_{L_k}}{C_a \cdot |Z_k(j \cdot \omega_s)|^2}, K_7 = \frac{V_d \cdot V_q}{C_a \cdot V_{d_{c_a}}^2} - \frac{K_a^2 \cdot R_{L_k}}{C_a \cdot |Z_k(j \cdot \omega_s)|^2},$$

$$K_8 = \frac{a_{tr} \cdot K_a \cdot K_b}{C_a \cdot |Z_k(j \cdot \omega_s)|} \cdot \sin(\varphi - \sigma), K_9 = \frac{I_d}{C_a \cdot V_{d_{c_a}}}, K_{10} = \frac{V_{C_{a2}} + V_{C_{a3}}}{C_a \cdot V_{d_{c_a}}},$$

$$K_{11} = \frac{V_{C_{a3}}}{C_a \cdot V_{d_{c_a}}}, K_{12} = \frac{a_{tr} \cdot K_a \cdot K_b \cdot V_{d_{c_b}}}{C_a \cdot |Z_k(j \cdot \omega_s)|} \cdot \sin(\varphi + v), K_{13} = \frac{V_{C_{a1}}}{C_a \cdot V_{d_{c_a}}},$$

$$K_{14} = \frac{V_{C_{a1}} + V_{C_{a2}}}{C_a \cdot V_{d_{c_a}}}, K_{15} = 2 \cdot \frac{K_a^2 \cdot R_{L_k} \cdot V_{d_{c_a}}}{C_b \cdot V_{d_{c_b}} \cdot |Z_k(j \cdot \omega_s)|^2} - \frac{a_{tr} \cdot K_a \cdot K_b}{C_b \cdot |Z_k(j \cdot \omega_s)|} \cdot \sin(\varphi - \sigma),$$

$$K_{16} = \frac{V_{d_{c_a}}^2 - R_{c_a} \cdot V_d \cdot V_q}{C_a \cdot R_{c_a} \cdot V_{d_{c_a}}^2} + \frac{K_a^2 \cdot R_{L_k}}{C_a \cdot |Z_k(j \cdot \omega_s)|^2}, K_{17} = \frac{P_{R_{L_k}}}{C_b \cdot V_{d_{c_b}}^2} + \frac{K_a^2 \cdot R_{L_k} \cdot V_{d_{c_a}}^2}{C_b \cdot V_{d_{c_b}}^2 \cdot |Z_k(j \cdot \omega_s)|^2},$$

$$K_{18} = \frac{1}{C_b}, K_{19} = \frac{V_{C_{b2}} + V_{C_{b3}}}{C_b \cdot V_{d_{c_b}}}, K_{20} = \frac{V_{C_{b3}}}{C_b \cdot V_{d_{c_b}}}, K_{21} = \frac{a_{tr} \cdot K_a \cdot K_b \cdot V_{d_{c_a}}}{C_b \cdot |Z_k(j \cdot \omega_s)|} \cdot \sin(\varphi + v),$$

$$K_{22} = \frac{V_{C_{b1}}}{C_b \cdot V_{d_{c_b}}}, K_{23} = \frac{V_{C_{b1}} + V_{C_{b2}}}{C_b \cdot V_{d_{c_b}}}, K_{24} = \frac{1}{L_{dc}}, K_{25} = \frac{R_{dc}}{L_{dc}}$$

$$G_{v_{dca}}(s) = \frac{V_{d_{c_a}}(s)}{I_d(s)} \Big|_{Y(s)=0} =$$

$$= -3 \cdot K_4 \cdot \frac{(s + K_1 - \frac{K_2 \cdot K_5}{K_4}) \cdot (s + K_{16}) \cdot (s^2 + (K_{16} \cdot K_{25} + 2 \cdot K_{17}) \cdot s + (2 \cdot K_{17} \cdot K_{25} + K_{18} \cdot K_{24}))}{(s + K_1) \cdot (s + K_{16}) \cdot (s^2 + (K_{16} \cdot K_{25} + 2 \cdot K_{17}) \cdot s + (2 \cdot K_{17} \cdot K_{25} + K_{18} \cdot K_{24})) \cdot (s + K_{16} - 2 \cdot K_{17}) - 9 \cdot K_8 \cdot K_{15} \cdot (s + K_{25})}$$

$$\forall Y(S) \in \{V_q(S), V_d(S), I_2(S), I_{2a}(S), I_3(S), I_{3a}(S), \varphi(S), V_{B1}(S), V_{B2}(S), V_{B3}(S), I_{2b}(S), I_{3b}(S), \}$$

$$C_{v_{dca}}(s) = G_{c_{\infty}} \cdot \left(1 + \frac{\omega_L}{s}\right)$$

$$\left\{ \begin{aligned} G_{c_{\infty}} &= -\frac{\sqrt{B^2 \cdot \frac{\omega_s^4}{\omega_{p1} \cdot \omega_{p4}} + A^2 \cdot \frac{\omega_s^{10}}{\omega_{p1} \cdot \omega_{p3} \cdot \omega_{p4} \cdot (\rho^2 + \zeta^2)}}}{k_u \cdot \frac{\omega_s^4}{\omega_{z1} \cdot \omega_{z2} \cdot (\rho^2 + \zeta^2)}} \\ k_u &= 3 \cdot \frac{K_4}{K_8 \cdot K_{15}} \cdot \left(\frac{\omega_{z1}}{\omega_{p1} \cdot \omega_{p3} \cdot \omega_{p4}}\right) \\ A &= (9 \cdot K_8 \cdot K_{15} \cdot \omega_{p4})^{-1}, B = (\omega_{p2} \cdot \omega_{p3} \cdot (\rho^2 + \zeta^2))^{-1} \\ \omega_{z1} &= K_1 - \frac{K_2 \cdot K_5}{K_4}, \omega_{z2} = \omega_{p2} = K_{16} \\ \omega_{p1} &= K_1, \omega_{p3} = K_{16} - 2 \cdot K_{17}, \omega_{p4} = K_{25} \\ \rho &= \frac{1}{2} \cdot (K_{16} \cdot K_{25} + 2 \cdot K_{17}) \\ \zeta &= \sqrt{2 \cdot K_{17} \cdot K_{25} + K_{18} \cdot K_{24}} \end{aligned} \right. \tag{A9}$$

$$G_d(s) = G_q(s) = G_{dq}(s) = \frac{I_d(s)}{V_d(s)} = \frac{I_q(s)}{V_q(s)} = k_{dq} \cdot \frac{s + \zeta \cdot \omega_n}{s^2 + 2 \cdot \zeta \cdot \omega_n + \omega_n^2}$$

$$\left\{ \begin{array}{l} \tau_{ac} = \frac{L_{ac}}{R_{ac}} \\ X_{ac}(j \cdot \omega) = \omega \cdot L_{ac} \\ Z_{ac}(j \cdot \omega) = R_{ac} + j \cdot X_{ac}(j \cdot \omega) \\ |Z_{ac}(j \cdot \omega)| = \sqrt{R_{ac}^2 + X_{ac}(j \cdot \omega)^2} \\ k_{dq} = \frac{1}{L_{ac}} \\ \omega_n = k_u \cdot |Z_{ac}(j \cdot \omega)| \\ \zeta = \frac{1}{\tau_{ac} \cdot \omega_n} \\ G_{c\infty} = \frac{\omega_s \cdot \zeta}{\omega_s \cdot k_u} \\ \omega_z = \omega_n \cdot \zeta \\ \omega_{p1,2} = \omega_n \cdot \left( -\zeta \pm j \cdot \sqrt{1 - \zeta^2} \right) \\ k_u = \frac{k_{dq} \cdot \omega_z}{\omega_{p1} \cdot \omega_{p2}} \end{array} \right. \tag{A10}$$

$$G_{C_{a_{imb2}}}(s) = \frac{V_{C_{a_{imb2}}}(s)}{I_2(s)} = G_{C_{a_{imb3}}}(s) = \frac{V_{C_{a_{imb3}}}(s)}{I_3(s)} = G_{C_{a_{imb}}}(s) = -\frac{\frac{1}{C_a}}{s + \frac{1}{R_{C_a} \cdot C_a}}$$

$$G_{c\infty} = \omega_s \cdot C_a \tag{A11}$$

$$\left\{ \begin{array}{l} G_{C_{b_{imb2}}}(s) = \frac{I_{DM2}(s)}{I_2(s)} = \frac{K_{24} \cdot (K_{19} + K_{22})}{(s + \omega_{p1}) \cdot (s + \omega_{p2})} \\ G_{C_{b_{imb3}}}(s) = \frac{I_{DM3}(s)}{I_3(s)} = -\frac{K_{24} \cdot (K_{23} - K_{20})}{(s + \omega_{p1}) \cdot (s + \omega_{p2})} \\ \omega_{p1,2} = -\frac{K_{16} - K_{17} + K_{25}}{2} \pm \end{array} \right. \tag{A12}$$

$$\pm j \cdot \sqrt{\frac{(K_{16} - K_{17} + K_{25})^2}{4} - K_{25} \cdot (K_{16} - K_{17}) - K_{18} \cdot K_{24}}$$

$$G_{c\infty} = \frac{\omega_s^2}{k_u} \cdot \left( \frac{1}{\omega_{p1} \cdot \omega_{p2}} \right)$$

$$G_\phi(s) = \frac{I_{CM}(s)}{\phi(s)} = k_{cm} \cdot \frac{s + \omega_z}{s^3 + a_2 \cdot s^2 + a_1 \cdot s + a_0}$$

$$\left\{ \begin{array}{l} \omega_z = K_6 - 2 \cdot K_7 - 3 \cdot \frac{K_{12} \cdot K_{15}}{K_{21}} \\ a_2 = K_6 + K_{16} + K_{25} \\ a_1 = (K_{16} + 2 \cdot K_{17}) \cdot (K_6 - 2 \cdot K_{17}) - 9 \cdot K_8 \cdot K_{15} + K_{18} \cdot K_{24} + K_{25} \cdot (K_{16} + K_{16}) \\ a_0 = K_{25} \cdot (K_{16} + 2 \cdot K_{17}) \cdot (K_6 - 2 \cdot K_{17} - 9 \cdot K_8 \cdot K_{15}) + K_{15} \cdot K_{24} \cdot (K_6 - 2 \cdot K_{17}) \\ k_{cm} = K_{21} \cdot K_{24} \end{array} \right. \tag{A13}$$

**References**

1. Razmjoo, A.; Ghazanfari, A.; Jahangiri, M.; Franklin, E.; Denai, M.; Marzband, M.; Astiaso Garcia, D.; Maheri, A. A Comprehensive Study on the Expansion of Electric Vehicles in Europe. *Appl. Sci.* **2022**, *12*, 11656. [CrossRef]
2. Acharige, S.S.G.; Haque, M.E.; Arif, M.T.; Hosseinzadeh, N.; Hasan, K.N.; Oo, A.M.T. Review of Electric Vehicle Charging Technologies, Standards, Architectures, and Converter Configurations. *IEEE Access* **2023**, *11*, 41218–41255. [CrossRef]
3. Dar, A.R.; Haque, A.; Khan, M.A.; Kurukuru, V.S.B.; Mehruz, S. On-Board Chargers for Electric Vehicles: A Comprehensive Performance and Efficiency Review. *Energies* **2024**, *17*, 4534. [CrossRef]
4. Vadi, S.; Bayindir, R.; Colak, A.M.; Hossain, E. A Review on Communication Standards and Charging Topologies of V2G and V2H Operation Strategies. *Energies* **2019**, *12*, 3748. [CrossRef]
5. Menyhart, J. Electric Vehicles and Energy Communities: Vehicle-to-Grid Opportunities and a Sustainable Future. *Energies* **2025**, *18*, 854. [CrossRef]

6. Rehman, M.A.; Numan, M.; Tahir, H.; Rahman, U.; Khan, M.W.; Iftikhar, M.Z. A Comprehensive Overview of Vehicle to Everything (V2X) Technology for Sustainable EV Adoption. *J. Energy Storage* **2023**, *74*, 109304. [[CrossRef](#)]
7. Gschwendtner, C.; Sinsel, S.R.; Stephan, A. Vehicle-to-X (V2X) Implementation: An Overview of Predominate Trial Configurations and Technical, Social and Regulatory Challenges. *Renew. Sustain. Energy Rev.* **2021**, *145*, 110977. [[CrossRef](#)]
8. Mojumder, M.R.H.; Ahmed Antara, F.; Hasanuzzaman, M.; Alamri, B.; Alsharef, M. Electric Vehicle-to-Grid (V2G) Technologies: Impact on the Power Grid and Battery. *Sustainability* **2022**, *14*, 13856. [[CrossRef](#)]
9. Dong, Z.; Tao, Y.; Lai, S.; Wang, T.; Zhang, Z. Powering Future Advancements and Applications of Battery Energy Storage Systems Across Different Scales. *Energy Storage Appl.* **2025**, *2*, 1. [[CrossRef](#)]
10. Chavhan, S.; Mohale, V.; Kumbhar, M. A Review of Recent Advancements and Challenges in Battery Energy Storage System (BESS). In Proceedings of the International Conference on Innovative Sustainable Technologies for Energy, Mechatronics and Smart Systems (ISTEMS), Dehradun, India, 26–27 April 2024; Institute of Electrical and Electronics Engineers Inc.: Piscataway, NJ, USA, 2024.
11. Wang, P.; Lu, J.; Wu, Y.; Xu, L.; Li, J.; Mao, H.; Tian, Y.; Xu, B.; Huang, J. A Novel Cooperative Control for SMES/Battery Hybrid Energy Storage in PV Grid-Connected System. *IEEE Trans. Appl. Supercond.* **2024**, *34*, 1–5. [[CrossRef](#)]
12. Khaligh, A.; Dantonio, M. Global Trends in High-Power On-Board Chargers for Electric Vehicles. *IEEE Trans. Veh. Technol.* **2019**, *68*, 3306–3324. [[CrossRef](#)]
13. Tu, H.; Feng, H.; Srdic, S.; Lukic, S. Extreme Fast Charging of Electric Vehicles: A Technology Overview. *IEEE Trans. Transp. Electrification* **2019**, *5*, 861–878. [[CrossRef](#)]
14. Rivera, S.; Kouro, S.; Vazquez, S.; Goetz, S.M.; Lizana, R.; Romero-Cadaval, E. Electric Vehicle Charging Infrastructure: From Grid to Battery. *IEEE Ind. Electron. Mag.* **2021**, *15*, 37–51. [[CrossRef](#)]
15. Rivera, S.; Goetz, S.M.; Kouro, S.; Lehn, P.W.; Pathmanathan, M.; Bauer, P.; Mastromauro, R.A. Charging Infrastructure and Grid Integration for Electromobility. *Proc. IEEE* **2022**, *111*, 371–396. [[CrossRef](#)]
16. Sakr, N.; Sadarnac, D.; Gascher, A. A Review of On-Board Integrated Chargers for Electric Vehicles. In Proceedings of the 2014 16th European Conference on Power Electronics and Applications, EPE-ECCE Europe, Lappeenranta, Finland, 26–28 August 2014. [[CrossRef](#)]
17. Metwly, M.Y.; Abdel-Majeed, M.S.; Abdel-Khalik, A.S.; Hamdy, R.A.; Hamad, M.S.; Ahmed, S. A Review of Integrated On-Board EV Battery Chargers: Advanced Topologies, Recent Developments and Optimal Selection of FSCW Slot/Pole Combination. *IEEE Access* **2020**, *8*, 85216–85242. [[CrossRef](#)]
18. Singh, A.R.; Vishnuram, P.; Alagarsamy, S.; Bajaj, M.; Blazek, V.; Damaj, I.; Rathore, R.S.; Al-Wesabi, F.N.; Othman, K.M. Electric Vehicle Charging Technologies, Infrastructure Expansion, Grid Integration Strategies, and Their Role in Promoting Sustainable e-Mobility. *Alex. Eng. J.* **2024**, *105*, 300–330. [[CrossRef](#)]
19. Wouters, H.; Martinez, W. Bidirectional Onboard Chargers for Electric Vehicles: State-of-the-Art and Future Trends. *IEEE Trans. Power Electron.* **2024**, *39*, 693–716. [[CrossRef](#)]
20. De Doncker, R.W.A.A.; Divan, D.M.; Kheraluwala, M.H. A Three-Phase Soft-Switched High-Power-Density DC/DC Converter for High-Power Applications. *IEEE Trans. Ind. Appl.* **1991**, *27*, 63–73. [[CrossRef](#)]
21. Alonso, A.R.; Sebastian, J.; Lamar, D.G.; Hernando, M.M.; Vazquez, A. An Overall Study of a Dual Active Bridge for Bidirectional DC/DC Conversion. In Proceedings of the IEEE Energy Conversion Congress & Exposition (ECCE), Atlanta, GA, USA, 12–16 September 2010; pp. 1129–1135. [[CrossRef](#)]
22. Filba-Martinez, A.; Busquets-Monge, S.; Nicolas-Apruzzese, J.; Bordonau, J. Operating Principle and Performance Optimization of a Three-Level NPC Dual-Active-Bridge DC-DC Converter. *IEEE Trans. Ind. Electron.* **2016**, *63*, 678–690. [[CrossRef](#)]
23. Campos-Salazar, J.M.; Busquets-Monge, S.; Filba-Martinez, A.; Alepuz, S. Multibattery Charger System Based on a Three-Level Dual-Active-Bridge Power Converter. In Proceedings of the IECON 2021—47th Annual Conference of the IEEE Industrial Electronics Society, Toronto, ON, Canada, 13–16 October 2021. [[CrossRef](#)]
24. Campos-Salazar, J.M.; Busquets-Monge, S.; Filba-Martinez, A.; Alepuz, S. Comparison of Modulations and Dc-Link Balance Control Strategies for a Multibattery Charger System Based on a Three-Level Dual-Active-Bridge Power Converter. In Proceedings of the 2022 IEEE 31st International Symposium on Industrial Electronics (ISIE), Anchorage, AK, USA, 1–3 June 2022; pp. 366–373. [[CrossRef](#)]
25. Filbà Martínez, À. Contributions to the Modulation and Closed-Loop Control of Multilevel Dual-Active-Bridge Dc-Dc Converters. Ph.D. Thesis, Universitat Politècnica de Catalunya, Barcelona, Spain, 2017.
26. Leon, J.I.; Vazquez, S.; Franquelo, L.G. Multilevel Converters: Control and Modulation Techniques for Their Operation and Industrial Applications. *Proc. IEEE* **2017**, *105*, 2066–2081. [[CrossRef](#)]
27. Busquets-Monge, S.; Filba-Martinez, A.; Alepuz, S.; Nicolas-Apruzzese, J.; Luque, A.; Conesa-Roca, A.; Bordonau, J. Multibattery-Fed Neutral-Point-Clamped DC-AC Converter with SoC Balancing Control to Maximize Capacity Utilization. *IEEE Trans. Ind. Electron.* **2020**, *67*, 16–27. [[CrossRef](#)]

28. Busquets-Monge, S.; Maheshwari, R.; Nicolas-Apruzzese, J.; Lupon, E.; Munk-Nielsen, S.; Bordonau, J. Enhanced DC-Link Capacitor Voltage Balancing Control of DC-AC Multilevel Multileg Converters. *IEEE Trans. Ind. Electron.* **2015**, *62*, 2663–2672. [[CrossRef](#)]
29. El Ghossein, N.; Salameh, J.P.; Karami, N.; El Hassan, M.; Najjar, M.B. Survey on Electrical Modeling Methods Applied on Different Battery Types. In Proceedings of the IEEE International Conference on Technological Advances in Electrical, Electronics and Computer Engineering (TAECE), Beirut, Lebanon, 29 April–1 May 2015; IEEE: Piscataway, NJ, USA, 2015; pp. 39–44.
30. Chen, M.; Rincón-Mora, G.A. Accurate Electrical Battery Model Capable of Predicting Runtime and I–V Performance. *IEEE Trans. Energy Convers.* **2006**, *21*, 504–511. [[CrossRef](#)]
31. Wenzl, H. BATTERIES | Capacity. In *Encyclopedia of Electrochemical Power Sources*; Elsevier: Amsterdam, The Netherlands, 2009; pp. 395–400, ISBN 978-0-444-52745-5.
32. Bacha, S.; Munteanu, I.; Bratcu, A.I. *Power Electronic Converters Modeling and Control*; Advanced Textbooks in Control and Signal Processing; Springer: London, UK, 2014; ISBN 978-1-4471-5477-8.
33. Rashid, M.H. *Power Electronics Handbook*; Butterworth-Heinemann: Oxford, UK, 2024; ISBN 9780323993432.
34. Ogata, K. *Modern Control Engineering*; Pearson: Boston, MA, USA, 2010.
35. Kuo, B.C. *Automatic Control Systems*; Prentice Hall: Englewood Cliffs, NJ, USA, 1991; ISBN 978-0-13-051046-4.
36. Levine, W.S. *The Control Handbook*, 2nd ed.; CRC Press: Boca Raton, FL, USA, 2018; ISBN 9781420073676.
37. Skogestad, S.; Postlethwaite, I. *Multivariable Feedback Control: Analysis and Design*, 2nd ed.; Wiley: Chichester, UK, 2005; ISBN 978-0-470-01167-6.
38. Campos-Salazar, J.M. Design and Analysis of Battery Chargers for Electric Vehicles Based on Multilevel Neutral-Point-Clamped Technology. Ph.D. Thesis, Universitat Politècnica de Catalunya, Barcelona, Spain, 2024.
39. Busquets-Monge, S.; Bordonau, J.; Boroyevich, D.; Somavilla, S. The Nearest Three Virtual Space Vector PWM—A Modulation for the Comprehensive Neutral-Point Balancing in the Three-Level NPC Inverter. *IEEE Power Electron. Lett.* **2004**, *2*, 11–15. [[CrossRef](#)]
40. Hayt, W.H.; Kemmerly, J.E.; Phillips, J.D.; Durbin, S.M. *Engineering Circuit Analysis*, 10th ed.; McGraw Hill, LLC.: New York, NY, USA, 2024; ISBN 1264149913.
41. Erickson, R.W.; Maksimović, D. *Fundamentals of Power Electronics*, 3rd ed.; Springer International Publishing: Cham, Switzerland, 2020; ISBN 978-3-030-43879-1.

**Disclaimer/Publisher’s Note:** The statements, opinions and data contained in all publications are solely those of the individual author(s) and contributor(s) and not of MDPI and/or the editor(s). MDPI and/or the editor(s) disclaim responsibility for any injury to people or property resulting from any ideas, methods, instructions or products referred to in the content.